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TFT Channel Materials for Display Applications: From Amorphous Silicon to Transition Metal Dichalcogenides

*Gi Woong Shim, Woonggi Hong, Jun-Hwe Cha, Jung Hwan Park, Keon Jae Lee, and Sung-Yool Choi**

As the need for super-high-resolution displays with various form factors has increased, it has become necessary to produce high-performance thin-film transistors (TFTs) that enable faster switching and higher current driving of each pixel in the display. Over the past few decades, hydrogenated amorphous silicon (a-Si:H) has been widely utilized as a TFT channel material. More recently, to meet the requirement of new types of displays such as organic light-emitting diode displays, and also to overcome the performance and reliability issues of a-Si:H, low-temperature polycrystalline silicon and amorphous oxide semiconductors have partly replaced a-Si:H channel materials. Basic material properties and device structures of TFTs in commercial displays are explored, and then the potential of atomically thin layered transition metal dichalcogenides as next-generation channel materials is discussed.

1. Introduction

1.1. History of Display Technology

As one of the most important human-computer interfaces that can output visual data in a readable form, displays have played a pivotal role in the rapid development of the Information Age. The first commercial display was a form of cathode ray tube (CRT), which was invented by F. Braun in 1897. Examples of these early displays include mechanical, electronic, and color televisions, which were first appeared in 1928, 1934, and 1953, respectively. In a CRT display, electrons are emitted from a cathode, and luminescence is generated when they collide with a phosphorescent screen in a vacuum tube. Even though CRT displays are inexpensive and simple in structure, they are inefficient in terms of power consumption and occupy much space.

Plasma display panels (PDPs) were first invented in 1927 using glow discharge to create images.[1] Current types of PDPs were first invented in 1964 and were commercially produced beginning in 1972. By 2010, PDPs up to 150 inches in size could be mass produced. In a PDP, ultraviolet (UV) light produced from plasma excites phosphors and generates light. Consequently, PDPs do not need backlight units, enabling them to cover wider color gamuts compared to those covered by liquid crystal displays (LCDs) using filters. In addition, because it is not necessary to rearrange liquid crystal (LC) molecules, PDPs exhibit a superior response rate compared to LCDs. Moreover, the structure of PDPs are simpler than LCDs that makes PDPs more advantageous in large-area scalability. However, because PDPs rely on glow discharge to operate, they consume large amounts of energy and produce a significant amount of heat. In addition, small PDP panels (<32 inches) have not yet been successfully produced. Therefore, LCDs and organic light emitting diodes (OLEDs) are widely used because of their energy efficiency and both small- and large-area scalability.

With regard to LCDs, electronic watches with LCDs were first produced in 1972, and active matrix-LCDs (AM-LCDs) containing high-temperature polysilicon (HTPS) came onto the market in 1984. Furthermore, AM-LCDs based on a-Si:H appeared in 1986, and in 2010 and 2012, respectively, AM-LCDs based on low-temperature polycrystalline silicon (LTPS) and amorphous oxide semiconductor (AOS) were produced. The first commercial use of OLEDs occurred in 1997 when passive matrix-OLEDs (PM-OLEDs) were incorporated into automotive audio systems. AM-OLEDs were first used in camera displays in 2003, and currently, ≈88 inch displays with 8K resolution that utilize both LCDs and OLEDs are widely used.

1.2. Driving Methods of Display

For low resolution displays such as those found on electronic watches, each electrode can be connected to a single pixel with a directly induced voltage input. This method is known as direct driving (**Figure 1**a). However, as the number of pixels increases into the range of about 10 000 pixels, the overall

G. W. Shim, W. Hong, J.-H. Cha, Prof. S.-Y. Choi
Graphene/2D Materials Research Center
Center for Advanced Materials Discovery towards 3D Display
School of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon 34141, Korea
E-mail: sungyool.choi@kaist.ac.kr
Dr. J. H. Park
Department of Mechanical Engineering
University of California
Berkeley, CA 94720, USA
Prof. K. J. Lee
Department of Materials Science and Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon 34141, Korea
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driving system becomes very complicated because there is now a need for 10 000 individual electrodes. Alternatively, the complexity of the driving system can be effectively decreased if the same 10 000 pixels are operated in a 100 × 100 matrix using an integrated circuit (IC) and timing controllers. Therefore, this matrix driving scheme has been extensively utilized in high resolution displays. There are two matrix driving methods, known as PM and AM. PM addressing is an addressing scheme in which scan lines in rows and data lines in columns are crossed and the overlapped area can be selected (Figure 1b). During a single time frame, the scan lines scan through the overall lines in serial order and then switch pixels on by applying voltage to the data lines. During this process, a single pixel stays on only during $1/n$ frame time (where n is the number of scan lines). Because luminance can be represented as an average of the brightness produced during the frame time, a high degree of brightness is momentarily necessary in each line, which creates disadvantages in terms of lifetime and power consumption (Figure 1d). Therefore, AM addressing, in which a constant lower level luminescence is maintained over one frame time, is preferred in high resolution displays. This is enabled by two processes. First, charges are stored in capacitors (C_{ST}) when the scan line turns on the switching TFTs by applying gate voltage. Then, the stored charges are used to supply voltage to the LC or the driving TFTs for the rest of the frame time (Figure 1c). Because AM addressing generates a lower luminance than PM addressing, it has a longer lifetime and consumes less power. In addition, it is possible to prevent crosstalk due to interference between the scan and data lines, which allows for a high contrast ratio and clear image outputs. However, for low resolution displays, the PM method without capacitors and TFTs has the advantage of being less expensive.

LCD uses a voltage driven driving scheme that operates by means of passing or blocking a backlight by applying voltage to easily polarizable LC molecules. In contrast, OLED normally adopts current driving methods, in which the luminance can be modulated depending on the current flow. For AM-LCD, a 1T-1C (1 transistor and 1 capacitor) structure is commonly used. However, AM-OLED works in 2T-1C structure in which the 2T elements consist of a driving transistor for tuning the current level and a switching transistor for turning it on or off (Figure 1c). In commercial displays, compensation circuits such as 6T-1C and 7T-1C are used to mitigate changes in materials properties and device characteristics over time, and to minimize issues due to non-uniformity of channel materials.[2]

To produce high resolution displays, the performance of TFTs needs to be improved. There are several advantages for using high mobility (μ) channel materials. First, in AM displays, high μ TFTs can guarantee that C_{ST} will be charged in a short amount of time. This is more preferred to drive displays with large panels, high resolutions, and high frame rates where the charging time allowed is very short.[3] Second, high μ TFTs are preferred when a high driving current level is needed. The driving current produced in TFTs depends on the geometry of channel. It is directly proportional to the channel width (W) and inversely proportional to the channel length (L). This implies that reducing L can be used to obtain a high current density. However, in current technology, L in display TFTs have already been reduced to 2–3 µm, which is close to the minimum size possible to produce using photolithography. Therefore, improving the intrinsic μ will boost the reduction in W further without causing degradation of the output current. This reduction in TFT size, in turn, contributes to decreased parasitic capacitance (undesired capacitance originated from the coupling between two components at a close distance;[4] components include electrodes and channels which can flow charges) and leads to the design of smaller-sized C_{ST}. Moreover, a reduction in the aperture ratio improves luminance and decreases power consumption.[5] Third, ultra-high-performance TFTs are required for applications demanding ultra-high resolutions such as mobile, augmented reality (AR), and virtual reality (VR) displays with various functionality and form factors. Finally, the high μ of TFTs enables peripheral circuits to be fabricated out of channel materials instead of using bulky IC chips.[6] This makes the design of thin bezels possible, which is preferable for esthetic reasons.

Figure 1e shows a typical transfer curve of TFTs. In the transfer curve, on current (I_{on}) and off current (I_{off}) are defined as the maximum and minimum currents that can be obtained by applying a gate bias. When operating the displays, I_{off} (or leakage current) is responsible for retaining charges in the

Gi Woong Shim received his B.S. degree in chemistry (2014) and M.S. degree in electrical engineering (2016) from Korea Advanced Institute of Science and Technology (KAIST). He is now pursuing a Ph.D. degree at KAIST under the supervision of Prof. Sung-Yool Choi. His research is focused on the multiphysics modeling of the growth system for high quality two-dimensional materials and its device applications.

Sung-Yool Choi received B.S., M.S., and Ph.D. degrees from the Department of Chemistry, Korea Advanced Institute of Science and Technology (KAIST), in 1991, 1994, and 1998, respectively. He worked as a senior/principal researcher at Electronics and Telecommunications Research Institute (ETRI) from 1998 to 2011, then he joined the faculty of the School of Electrical Engineering, KAIST. He now serves as a director of the Graphene/2D Materials Research Center (GRC) and the Center for Advanced Materials Discovery towards 3D Display (CAMD^3). His research focuses on the synthesis and processing of two-dimensional materials and their applications to the field of energy, electronics, and photonics.

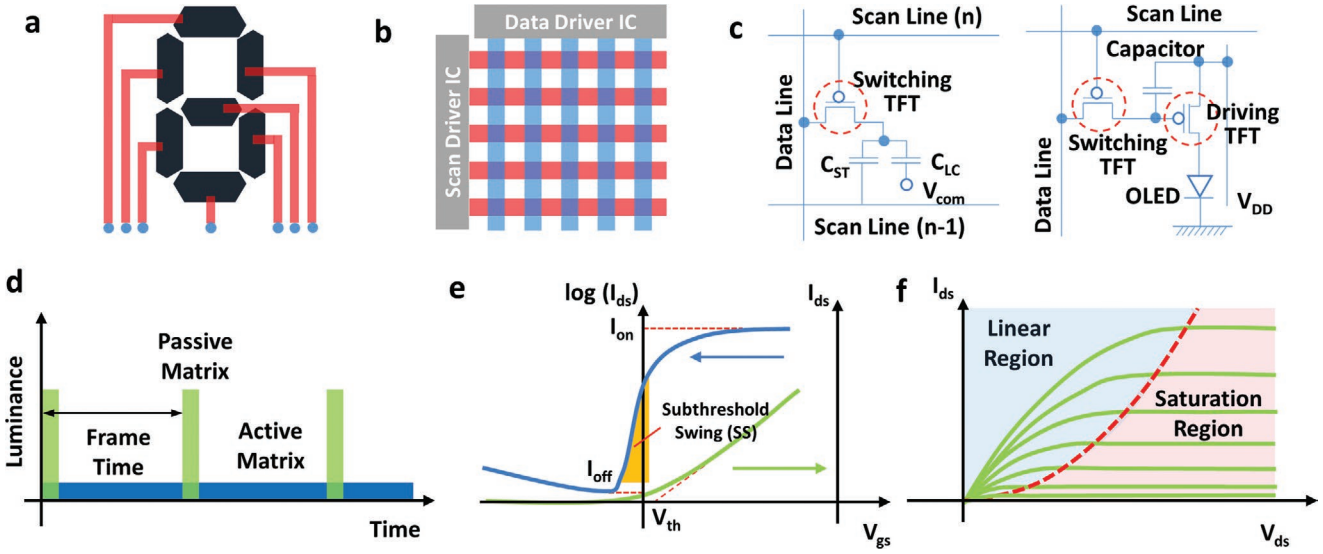

Figure 1. a) Direct driving scheme of display for number representation. b) PM addressing scheme of display. c) Typical circuit diagram for 1T-1C LCDs and 2T-1C OLEDs. C_{LC} and C_{ST} represent the capacitance from liquid crystals and the storage capacitor, respectively. V_{com} is the common voltage, and V_{DD} is the drain voltage of the DC power supply. d) Luminance change with time for PM and AM addressing during a frame time. e) Typical transfer curve for TFTs. I_{ds} represent the drain current. V_{gs} is the gate voltage, and V_{th} is extracted in the linear region. f) Typical output curve of the TFT. V_{ds} is the drain voltage.

C_{ST}. If I_{off} is large, the stored charges can be easily released. Therefore, the refresh rate should be high to compensate for these discharges, and this causes the power consumption to increase. I_{on} is especially important for driving OLED displays, which require a high driving current (10–100 mA cm^{-2}). For a display that has a pixel size of 100 × 100 μm^2, μ required for driving an OLED with 5 μA per pixel is estimated to be 12.5 cm^2 V^{-1} s^{-1}.[7] Subthreshold swing (SS) is defined as the gate voltage necessary to increase the drain current by a factor of 10 in the subthreshold region. In TFT, SS is related to the interfacial trap density (the smaller the interfacial trap density, the smaller the SS value). Having a smaller SS is advantageous for increasing the switching speed and reducing power consumption. Threshold voltage (V_{th}) is the minimum gate voltage necessary to allow current to flow in the TFT. Several extraction methods are available, but the extrapolation in the linear regime method is widely used (Figure 1e), where the V_{th} is represented as the sum of V at the intercept and $V_{ds}/2$.[8] V_{th} is related to the power consumption, and its polarity is important in the design of circuit. Figure 1f shows the output curve, which is divided into a linear region (blue) and a saturation region (red). Pinch-off voltage, which is the point at which an increase in drain bias does not contribute to additional current flow, is used to distinguish between the two regions. Switching TFTs in LCDs and OLEDs operate in the saturation region because the only function required is the ability to turn on and off. For driving TFTs in OLEDs, precise tuning of the current is needed, which means that they should operate in the linear region.

1.3. Requirements of TFT Processes and Substrates

TFT processes are normally carried out in a temperature range that extends up to 600 °C. Accordingly, substrates should be able to withstand these temperatures while still being affordable. Glass substrates are widely used, because they have advantages in terms of price, rigidity, and low-temperature processsability. In addition, in visible light (380–740 nm), glass substrates have a high transmittance of >90%, which is essential for backlight-based LCDs. As for OLEDs, such a high transmittance can achieve a high efficiency with a bottom emission structure. However, for a top emission structure, the substrate does not need to be transparent. Therefore, polymer substrates such as polyimide (PI) are also widely used for top emission OLED displays. Meanwhile, both glass and heat resistant polymer substrates need to have relatively flat and smooth surfaces with good thermal resistance and low thermal expansion coefficients. Moreover, a high stability for chemical exposure and low permeability to oxygen and water is required.

The low temperature processability requirement is more strict for channel materials within displays. Even though single crystal materials have higher μ, the area that can be achieved by a single crystal growth of silicon is limited to ≈12 inches (300 mm). Note that the temperature necessary for the silicon single crystal growth is also high due to its high melting point (1414 °C). Therefore, channel materials in the display are deposited as thin amorphous or poly-crystalline films by a vapor deposition process instead of as single crystals.

The concept of devices based on thin films, or TFT, was first patented in the 1930s,[9] and TFTs that used vacuum-deposited polycrystalline CdS were first reported in 1962.[10] Later, CdSe, Te, PbS, InSb, and PbTe, with μ ranging from several to several dozens of cm^2 V^{-1} s^{-1} were reported.[11] In 1971, the concept of operating LCs with an AM consisting of 1T-1C and one LC element was first proposed,[12] and based on this concept, the first CdSe-based AM-LCD was reported in 1973.[13] In 1979, TFTs using a-Si:H that was deposited by a glow discharge method were reported.[14] Meanwhile, compound semiconductors such as CdSe

were unable to be commercialized due to difficulties in controlling their properties and low device reliability in large areas.[15] In contrast, existing well-established Si-based processes have allowed for rapid commercialization of a-Si:H and LTPS technologies.

2. Hydrogenated Amorphous Si TFTs

2.1. Density of States of a-Si:H

To evaluate the potential of emerging channel materials such as transition-metal dichalcogenides (TMDCs), it is important to understand the traditional but commercialized channel materials such as a-Si:H and LTPS. It is because they are governed by similar physical principles (i.e., carrier transport models, density of states or DOSs, bias instability models). a-Si:H is deposited by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 as a precursor. Here, plasma is used to lower decomposition temperature of SiH_4 from ≈800 to ≈300 °C, and that the substrate can withstand.[16] However, due to the low deposition temperature, amorphous films with a short-range order are deposited (**Figure 2**a), showing significantly inferior characteristics over single crystal Si. Despite that, a-Si:H has an exceptionally good uniformity that it is widely used in both small and large-sized displays.

The electrical properties of a-Si:H are highly related with DOS. Figure 2b,c shows how DOS of crystalline Si (c-Si) and a-Si (or a-Si:H) is different. First, due to variations in bond length (Si–Si) and bond angle, the band gap is larger for a-Si. Also, tail states and deep states are present between the conduction band (CB) and the valence band (VB) with a non-negligible density.[17] Here, deep states are located far from both CB and VB edges and act as a deep trap site that capture charge carriers for a long time and severely degrade the transport properties of a-Si.[18] Since deep states originate from non-bonding states, hydrogenation by H_2 flow during PECVD is carried out to drastically reduce DOS of deep states from ≈5×10^{19} to 10^{15}–10^{16} cm^{-3} (red-dotted line in Figure 2c).[19] Carrier transport in a-Si:H at

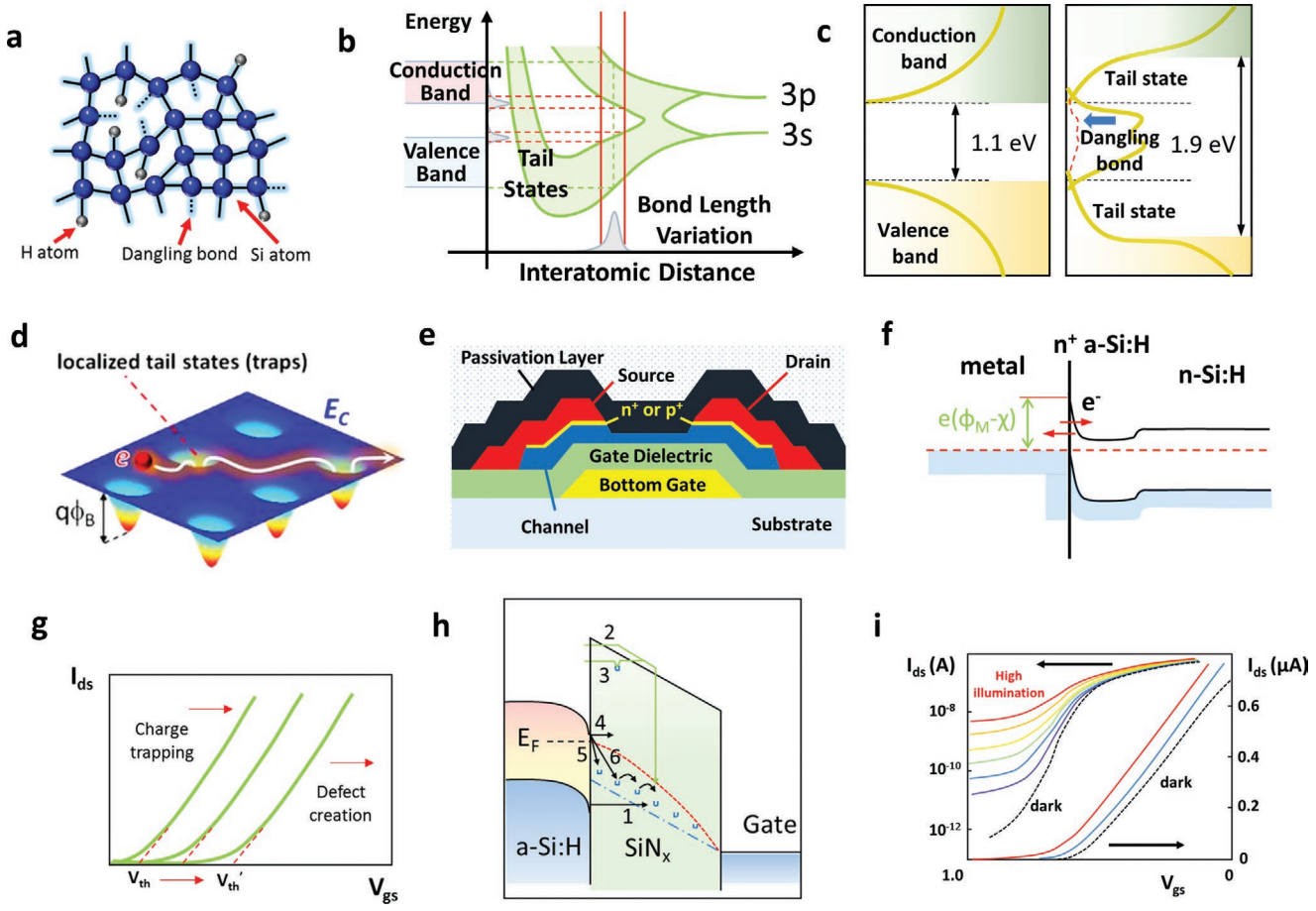

Figure 2. a) Schematic of the structure of a-Si:H in the presence of dangling bond (dotted line) and variation in Si–Si bond length. (b) Schematic showing how the DOS for a-Si can be constructed by favorable (bonding) and non-favorable (anti-bonding) interactions of the constituent orbitals of Si (3p and 3s). c) A comparison between the DOS of c-Si and a-Si (a-Si:H), showing the enlarged band gap and the formation of additional states (tail and deep states) in a-Si:H. d) Transport of electrons in the CB of Si by the trapping and detrapping mechanism. e) A typical structure of a bottom-gate, staggered, BCE type TFT. f) Band alignment at the interface of metal/n^+ a-Si:H/a-Si:H. χ stands for the electron affinity. g) Shift in the transfer curve due to the charge trapping and defect creation mechanism in a-Si:H. h) Schematic representation of the charge injection and trapping mechanism in a-Si:H TFTs by gate bias. i) Shift in the transfer curve at various levels of illuminations in a-Si:H. d) Reproduced with permission.[20b] Copyright 2015, Springer Nature. h) Reproduced with permission.[28] Copyright 1983, AIP Publishing LLC. i) Reproduced with permission.[33] Copyright 1985, Elsevier B.V.

the room temperature primarily occurs through the CB (electrons) or VB (holes) that are hampered by trapping at the tail states (Figure 2d).[20] Experimentally, drift μ is measured as 0.5–1 $cm^2\ V^{-1}\ s^{-1}$ for electrons and ≈0.01 $cm^2\ V^{-1}\ s^{-1}$ for holes.[21] The large difference in μ enables only n-channel metal oxide semiconductor (NMOS) transistors to be employed for a-Si:H TFTs.

2.2. Basic Device Structures

2.2.1. Bottom-gate, Staggered, Back Channel Etched Structure

TFT structures can be classified by the location of source, gate, and drain electrode. If the gate electrode is located under the semiconductor (or active layer), it is bottom-gated. For coplanar structure, source, drain, and gate electrodes are located on the same side of the active layer. On the other hand, staggered structure represents the gate electrode and source/drain electrode placed on the opposite sides of the active layer. Figure 2e shows a typical structure (bottom-gate, staggered, back channel etched or BCE) used in commercial a-Si:H TFTs. For driving a-Si:H TFTs, this structure has powerful advantages in sequential deposition of gate insulator (GI, a-SiN_x:H), channel (a-Si:H), and ohmic contact and hole blocking layer (n^+ a-Si:H) without breaking the vacuum during PECVD. This prevent the surface from being exposed to the ambient air during sequential deposition that minimize detrimental defect formation. This is especially important for a-Si:H, which is defect-rich and shows low performance. For staggered structure with the top-gate, sequential deposition is also possible. However, ohmic contact layer should be deposited first, which is not preferred since dopants can be incorporated to the active layer during the following deposition of a-Si:H.

Meanwhile, for bottom-gate staggered structure, deposition of source and drain electrodes should be carried out after deposition of trilayers (a-SiN_x:H, a-Si:H, and n^+ a-Si:H). Followed by the metal patterning, ohmic contact layer above the channel should be removed. This can be done by dry etching method, however, etching has no selectivity between ohmic and active layer.[22] If n^+ layer is not completely removed, leakage current can be increased. Therefore, over-etching of the n^+ a-Si:H layer takes place, which results in BCE structure. At this time, the a-Si:H layer is normally etched more than 10 nm. Therefore, the active layer should be sufficiently thick. When using etch stop layer (ESL) such as a-SiN_x:H instead of BCE structure, additional photomasks are needed.[23] Considering that the manufacturing cost largely increases with the number of masks, BCE structure is widely used in industry even if degradations in the properties (e.g., reduction in μ, increase in SS, etc.) of active layer can occur during dry etching process.

2.2.2. Heavily Doped Layers for Reduction in Contact Resistance

At the interface between metals and semiconductors, pinning of the Fermi level (E_F) of metals to the certain level within semiconductors is commonly observed.[24] This results in the formation of Schottky barriers regardless of the work function (φ) of metals. To solve this issue in Si electronics, heavily doped layers were introduced between metals and semiconductors.[25] When n^+ or p^+ region is introduced, Schottky barrier width can be effectively reduced. As a result, even though Schottky barrier is present, charge carriers can tunnel through the barrier and be injected into the semiconductor. Then, the ohmic contact can be formed and the contact resistance (R_c) can be mitigated (Figure 2f). The decrease in R_c reduces current crowding effects, which increases I_{on} and improves μ. Meanwhile, to achieve heavy doping, ion implantation is used in Si electronics. However, this is inefficient in a-Si:H due to low doping efficiency (the ratio of activated dopants to injected dopants) and the high density of tail states. Also, the subsequent annealing for the activation of dopants may remove hydrogen in a-Si:H, making plenty of deep trap states. Therefore, the doping in a-Si:H is performed by supplying dopant precursors together during the PECVD process for a-Si:H deposition. The final TFT devices show typically low I_{off} (≈10^{-12} A), which is attributed to the relatively high band gap of a-Si:H that prevent minority carriers generated by thermal energy.[26]

2.3. Bias Stress Instability

If the devices are operated for a prolonged time, device performance may degrade, or so-called device instability occurs. Among many parameters, instability of V_{th} is the most notable (Figure 2g). The two main mechanisms responsible for the instabilities in a-Si:H are charge trapping and creation of deep state (dangling bond).[18,27] First, applied field is screened by trapped charges at the GI/channel interface or within GI, resulting in the larger field required to achieve the same level of field within an active layer. Creation of deep states is caused by applied bias, which changes E_F of a-Si:H and results in occupation of tail states in a-Si:H that can break weak bond and create dangling bond. Here, the created defects are metastable since annealing can effectively restore the changes made by the created defects.

To explain the charge trapping, the model suggested by Powell is widely used.[28] Several routes are possible for the trapping as in Figure 2h. Experimentally, ΔV_{th} has very little dependency on temperature.[29] Therefore, the rate limiting step for charge trapping is tunneling (or injection of carriers from a-Si:H) rather than hopping within a-Si:H. Tunneling can take place in various routes, such as direct tunneling from states in a-Si:H to traps in SiN_x, or Fowler-Nordheim tunneling to CB in SiN_x followed by deep trapping (1–4 in Figure 2h). When the equilibrum among dangling bonds and related species are considered, ΔV_{th} by defect creation can be expressed as Equation (1), which shows power-law dependency with the time.

$$\Delta V_{th} = \left(V_{gs} - V_{th}\right)\left(t / t_0\right)^{\beta} \tag{1}$$

Libsch and Kanichi suggested stretched-exponential model to explain both charge trapping and defect creation when applying bias. This can be expressed as Equation (2).

$$\left|\Delta V_{th}\right| = \left|\Delta V_0\right|\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{2}$$

where the ΔV_0 is ΔV_{th} at infinite time, τ is the characteristic trapping time of carrier, and β ($0 < \beta \leq 1$) is the stretched-exponential exponent. Here, τ reflects how fast the trapping and detrapping processes occur and smaller value implies fast process.[30] Physically, τ is related with the energy barrier for the carrier injection from a-Si:H to SiN_x. And β means a degree of divergence from exponential function. When β is 1, charge trapping with the time shows narrow distribution while broader distribution is expected when β is <1. Thus, as β is close to 1, the distribution of trap state can be regarded as narrow.

At short time ($t < \tau$), low bias, and low temperature, $\exp(x)$ can be approximated as $1 + x$ ($x << 1$) by Taylor series. Therefore, Equation (2) converges to the Equation (1). This indicates that the carriers are trapped at the surface region of SiN_x, but are not diffuse further. On the other hand, at long time ($t > \tau$), high bias, and high temperature, trap states at the surface region of SiN_x is filled and further emission of carriers to trap states in bulk SiN_x occur. Meanwhile, Equation (2) cannot be approximated as Equation (1) since no further redistribution of trapped carriers with time is assumed for Equation (1).[31]

Not only bias stress at dark conditions but bias stress under illumination should be considered. In commercial displays, active layers are covered by blocking layers to hinder light from entering. However, some portion of scattered light can enter to the active layer. In a-Si:H, many tail states can be excited by light with ease and produce free carriers. This is favorable for a solar cell application, however, is detrimental to the TFT reliability. As a result of large absorption of light, a-Si:H typically shows high photo-conductivity.[32] Figure 2i shows bias stress instability under different level of illuminations, showing a shift in V_{th} and an increase in I_{off} for more than four orders of magnitude.[33] Meanwhile, due to the metastability of excited carriers,[34] the induced change of ΔV_{th} by charge trapping can be recovered by annealing.[35]

3. Low-Temperature Polysilicon TFT

3.1. Excimer Laser Annealing

To operate an LCD, the low μ of a-Si:H ranging from 0.5 to 1 $cm^2\ V^{-1}\ s^{-1}$ is sufficient. However, a-Si:H has a disadvantage in terms of its bias instability. Since an OLED is operated by means of current driving, subtle variations in V_{th} would change the current level and luminance significantly. Meanwhile, the role of LCD-TFT is to change direction of LCs, which requires relatively low current that the use of a-Si:H is sufficient. The light source of LCD is a backlight. On the other hand, OLED is based on light emitting organic molecules that collect holes and electrons and recombine them to emit light. The intensity of the emitted light should be comparable to that of backlight from LED. Thus, a high level of current is required to drive OLED-TFTs, which is hard to be achieved by using a-Si:H. Therefore, a new channel material with bias stability and high μ is required to drive OLED. Meanwhile, when a strong laser is irradiated on the a-Si surface, the surface temperature of <1300 K can be reached in a short time, which can melt the a-Si.[36] At this time, a-Si is crystallized into poly-Si owing to its energy stability. The crystallized LTPS now can show a high μ, typically ≈100 $cm^2\ V^{-1}\ s^{-1}$. It is also possible to crystallize by supplying large amount of thermal energy (≈1000 °C). Therefore, poly-Si can be produced through furnace annealing of a-Si:H, and the resulting poly-Si is called HTPS. However, there are critical limitations for using HTPS. Since glass and polymer substrates can withstand temperatures of up to ≈600 °C, high-temperature processable substrates such as quartz should be used. Because of using substrates with large thermal budget, processes such as gate oxidation and dopant activation can be carried out at high temperatures, which gives a high-quality poly-Si TFTs with their μ as high as 50 $cm^2\ V^{-1}\ s^{-1}$. Since the cost of the process increases rapidly as the size of the substrate grows, HTPS is an excellent choice in terms of price performance when the display size is small. Therefore, an HTPS-based application is limited to projector displays of ≈2–3 inches in size.[37]

In the case of LTPS, crystallization is achieved using a 305 nm XeCl excimer laser, which is called excimer laser annealing (ELA), as shown in **Figure 3**a. Here, the pulse width of the excimer laser is generally very small, such as several tens of nanoseconds. Therefore, the temperature is increased and quenched very rapidly by the transient heat diffusion, thereby avoiding thermal damage to the substrate located under the a-Si layer. In addition, to prevent the diffusion of mobile impurities contained in the substrate, SiO_x, SiN_x, or a multilayer film composed of these materials is deposited on the substrate. This layer is called buffer layer, and it also prevents diffusion of generated heat by ELA into the substrate. When laser is irradiated on the a-Si film, a gate electrode can melt if it is placed under a-Si. Therefore, top-gate structure is generally used for the LTPS.

Meanwhile, a laser with a point source is transformed into a linear shape through the use of a beam shaper and homogenizer. At this time, the size of the commercialized linear beam is ≈$1500 \times 0.4\ mm^2$ at most. The larger beam will be better in terms of uniformity. However, not only it is difficult to make the lens large, but a high maintenance cost is required to fill the source gas (e.g., Xe) and the large number of masks are required to realize top-gate, coplanar structures. Therefore, LTPS is not practical for the large-area display applications, and its majority use is in mobile display. In addition, since the laser intensity is extremely uneven at the end of the line beam, it is difficult to obtain uniform grain sizes through a single shot irradiation. Thus, multiple scanning of the laser beam of up to dozens of times are carried out. However, still there are limitations to increasing the grain size and improving the uniformity.[38] In addition, because the crystals have grain boundaries, large-area uniformity is inferior to that of a-Si:H or AOSs.

Figure 3b shows the sizes of the grains formed according to the energy density of the laser when irradiated with a single-pulse excimer laser. If the energy density is low, only the upper part of the a-Si layer is partially melted, and the latent heat emitted through the solidification of the melted a-Si repeats the melting of the a-Si underneath, causing an explosive crystallization up to a certain thickness.[36] This is called a partial melting regime. At this time, nucleation occurs at the interface between a-Si and molten Si. Since the crystallinity of the seed layer (i.e., a-Si layer) is poor, LTPS with high density of nuclei (i.e., small grain size) is formed. By contrast, when the

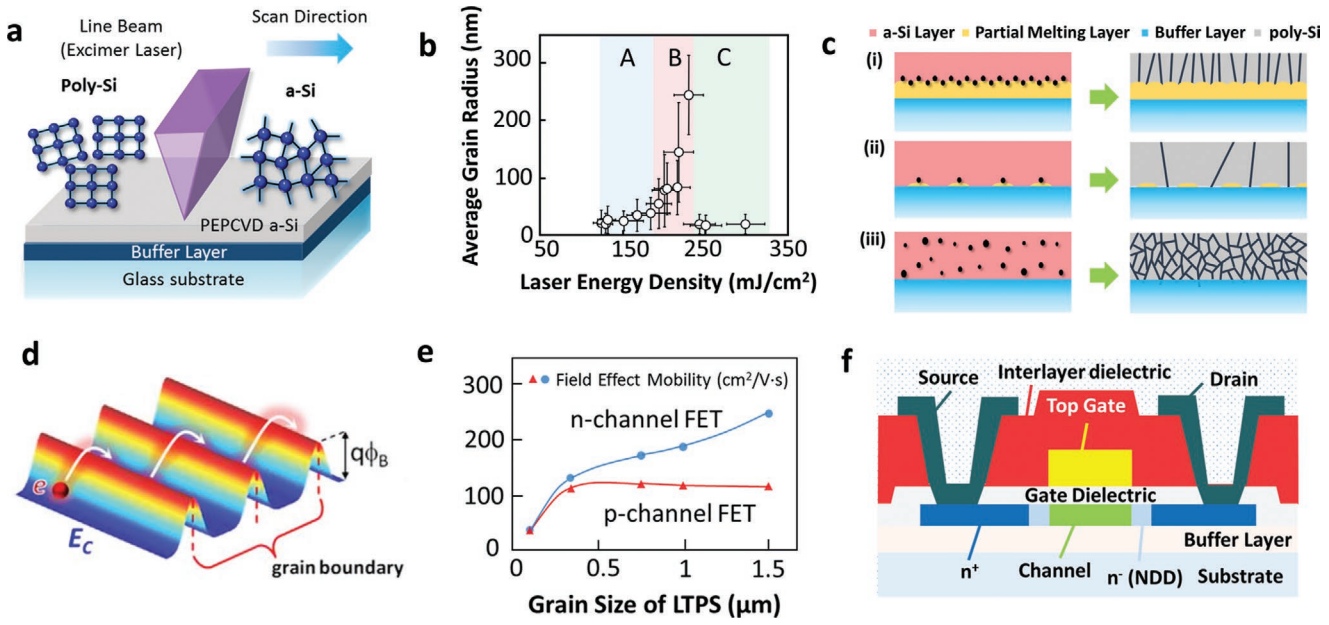

Figure 3. a) Schematic of ELA-induced phase transformation from a-Si to LTPS. b) Average grain size of ELA-LTPS with the energy density of the laser. c) Phase transformation mechanism with the energy density of the irradiated laser at partial melting, near-complete melting, and complete melting regime. d) Schematic of the transport of electrons in the CB of poly-Si experiencing barriers at the grain boundaries. e) Change in the n-channel and p-channel μ_{FE} of LTPS with grain size. f) Schematic of the top-gate, self-aligned, coplanar structure of LTPS. b) Reproduced with permission.[39] Copyright 1993, AIP Publishing LCC. d) Reproduced with permission.[20b] Copyright 2015, Springer Nature. e) Reproduced with permission.[40] Copyright 1999, Wiley-VCH.

energy density increases, a near complete melting regime is reached. At this time, a portion of the unmelted a-Si acts as a seed, resulting in nucleation, which greatly reduces the nucleation density and forms large grains.[39] When the energy density becomes higher, or under complete melting regime, all the a-Si layer melts and homogeneous nucleation occurs. Therefore, the nucleation density increases again, which barely changes even when the energy density increases. Therefore, practically ELA is carried out in a near complete melting regime (B and (ii) in Figure 3b,c). For the grain size, larger grains usually give high μ since the transport of charge carriers are highly hindered at the grain boundaries (Figure 3d). However, typical channel μ shows a saturation behavior when the grain size becomes greater than ≈1 μm (Figure 3e).[40]

3.2. Basic Device Structures

3.2.1. Top-gate, Coplanar, Self-Aligned Structure

To reduce the parasitic capacitance in LTPS, ion implantation is conducted using a gate electrode as a mask to form an n^+ or p^+ ohmic contact layer, and the dopant is activated through annealing in furnace or rapid thermal annealing (RTA). This structure is called a self-aligned structure (Figure 3f). In this case, because the gate electrode does not overlap with the source and drain electrodes, there is an advantage of reducing both the parasitic capacitance and the number of masks. Increasing the parasitic capacitance can lead to an RC delay and kick-back, which can be a source of quality degradation in display such as flickering.[41]

In terms of GIs, when the active layer is a-Si:H, TFTs with PECVD-SiN_x as GI generally exhibits better performance than that TFTs using PECVD-SiO_x as GI. For example, low bias stress instability and smaller SS is achieved when SiN_x was used as GI.[17] By contrast, the LTPS formed by the ELA process has an extremely poor roughness. Therefore, typically SiO_x is used as GI, which has a high quality and can form a good interface with Si.

Meanwhile, unlike a-Si:H, LTPS allows a complementary MOS (CMOS) technology to be implemented because the hole μ (μ_h) is comparable to the electron μ (μ_e), which can reduce the power consumption. However, there is a disadvantage in that the process cost increases owing to an increase in the number of masks. For an NMOS, it can perform better than PMOS because μ_e is higher than μ_h for an LTPS. However, PMOS can be implemented with ease since it has a lower leakage current and the TFT is connected to a stable ITO electrode in an OLED. By contrast, NMOS is more difficult to realize because the TFT should be connected to the cathode electrode, which is relatively unstable in an OLED.

3.2.2. Lightly Doped Drain Structure

Unlike a-Si:H, LTPS has a high μ_e. This enables acceleration of electrons at a high speed and leads to impact ionization. As a result, an additional electron-hole pairs are generated, and the high energy of the hot carriers can damage the active layer and GI, creating interface states. As a result, when a reverse bias is applied, the trapped minority carriers can flow that leads to a high leakage current. If the leakage current is high, the charge

stored in the capacitor is consumed constantly even if the pixel is not in an on-state. Therefore, power consumption should be increased to compensate for this. In addition, if the number of carriers increases drastically through an impact ionization, a kink occurs, in which the I_{ds} does not remain constant and increases rapidly as the V_{ds} increases in the saturated region. This leads to an instability of V_{th}. Eventually, the problems can be improved by reducing the electric field near the drain electrode. The simplest approach is to increase the distance between the drain electrode and the channel, which can reduce I_{off} but increase the parasitic resistance (a parasitic capacitance originates from a capacitor, which always has a resistance[42]), which can significantly reduce I_{on}. As a result, I_{on}/I_{off} remains similar.[43] To compensate for this, weakly doping (n^-) the offset region between the drain electrode and the channel was devised.[43,44] This method is called a lightly doped drain (LDD), in which the parasitic resistance decreases and the drain field increases with the doping concentration. Therefore, a moderately low doping concentration results in a low drain field and low parasitic resistance, thereby reducing I_{off} while maintaining I_{on} at a similar level.[43] Hatano et al. reported that when LDD structure is introduced, I_{on} in the NMOS and PMOS are similar but I_{off} decreases by an order of ≈1. Also, the kink current was suppressed.[45]

3.2.3. Dual and Asymmetric (L- or U-Shaped) Gate Structure

Increasing the number of gates between the source and drain electrodes simply divides the voltage between them and reduces the drain field, thus reducing the leakage current and suppressing the kink phenomenon. According to Proano et al., as the number of gates in LTPS TFT increases from 1 to 6, I_{on} decreases by approximately one order, whereas the leakage current decreases by two to three orders.[46] At this time, the distances between the gates are equal. Then V_{ds} voltage distribution along each gate varies according to the gate bias. Therefore, to optimize the voltage division, an asymmetric gate structure may be used that varies the distance between gates in a multiple gate structure.[47] In the case of commercial LTPS TFTs, L- or U-shaped gates are frequently used considering non-uniformity in grain sizes and properties in LTPS.[48] Shin et al. showed that when an L-shaped dual-gate structure is used in sequential lateral solidification (SLS)-LTPS, I_{ds} showed a level between the horizontally connected and the vertically connected dual-gate TFT. Also, kink current was significantly decreased.[49]

4. Amorphous Oxide Semiconductor TFTs

4.1. Conduction Mechanism in Amorphous Oxide Semiconductors

4.1.1. Origin of High Conductivity

As mentioned in Section 2.1, the low μ originated from the absence of long-range ordering in a-Si:H made the use of a-Si:H impractical for high-end displays. LTPS, on the other hand, has much improved crystallinity (≈μm of grain size) and thus has high μ (≈100 $cm^2\ V^{-1}\ s^{-1}$). However, poor uniformity and cost issues hindered LTPS from being used in large-area displays. Therefore, there have been demands on new high μ materials having both high μ and large-area scalability. Meanwhile, for the past decades, there has been numerous efforts on discovering transparent and amorphous oxides but having high μ. An important starting point of this effort was a work done by Hosono et al. in the 1990s.[50] Their initial guess was that amorphous materials with a high conductivity should satisfy the following condition: The overlap between CB orbitals are large while the magnitude of overlap is insensitive to structural randomness. They found that heavy metal cation with the electronic configuration in a form of $(n\text{-}1)d^{10}ns^0$ can satisfy these conditions. Also, to ensure amorphous nature, they evaluated electrical properties of double oxides (Cd_2GeO_4, $AgSbO_3$, etc.) rather than single oxides. However, the Hall μ was typically low. To achieve high μ (≈10 $cm^2\ V^{-1}\ s^{-1}$), additional processes such as Li^+ or H^+ implantation, or annealing below crystallization temperature (≈500 °C for a-IGZO) at O_2 atmosphere were required.

Many compounds containing metal-oxygen bonds are classified as ionic oxides. To give an example of IGZO, Pauling electronegativity (*EN*) is 1.78 for In and 3.44 for O. Thus, large difference in *EN* provides ionic nature in IGZO.[51] In the case of In_2O_3, a stoichiometric compound of In ([Kr] $4d^{10}5s^25p^1$) and O ([He] $2s^22p^4$) can be regarded as a compound from In^{3+} ion ([Kr] $4d^{10}$) and O^{2-} ion ([Ar]). Therefore, it is plausible that CB is mainly composed of 5s orbitals while 2p orbitals consist of VB. Here, the size of 5s orbitals is much larger than that of 2p orbitals. Given that the diameter of the s orbitals is larger than the distance between the cations, overlap between adjacent s orbitals can occur (**Figure 4**a).[52] Moreover, s orbitals has spherical shape that is highly isotropic. This makes large overlap between s orbitals possible without having long-range ordering, and results in high μ_e by conduction of carriers through CB. Also, much deeper level of O 2p orbitals compared to In 5s orbitals give rise to a large band gap of ≈3.1 eV and a very low I_{off} compared to a-Si:H. Due to the band gap larger than visible light (380–740 nm or 1.7–3.3 eV), it shows high transparency.

In 2004, Hosono group finally succeeded to discover a-IGZO (a-$InGaZnO_4$) with high μ of ≈10 $cm^2\ V^{-1}\ s^{-1}$.[52] IGZO film was prepared by pulsed laser deposition (PLD) using $InGaZnO_4$ target and under O_2 atmosphere at room temperature, and did not undergo further processes such as annealing. PLD is preferred in terms that the stoichiometric transfer of target is possible, however, not suitable for large-scale production. Nowadays, for the mass production, a-IGZO or AOSs are deposited at room temperature in O_2 atmosphere by sputtering using IGZO target. Targets are usually prepared from sintering of oxide mixtures (e.g., In_2O_3-Ga_2O_3-ZnO).[53] AOS-based TFTs had the advantages that they could utilize previously installed lines that were designed to fabricate bottom-gate staggered structure of a-Si:H TFTs. Being amorphous in nature, AOSs are also suitable for large-scale applications that require uniformity. Also, in terms of manufacturing costs, sputtering is better than ELA. Moreover, preparation of high-quality sputtering targets can be done with ease. Therefore, AOS-based display was realized in a very short time as compared with a-Si:H and LTPS.[54] Since

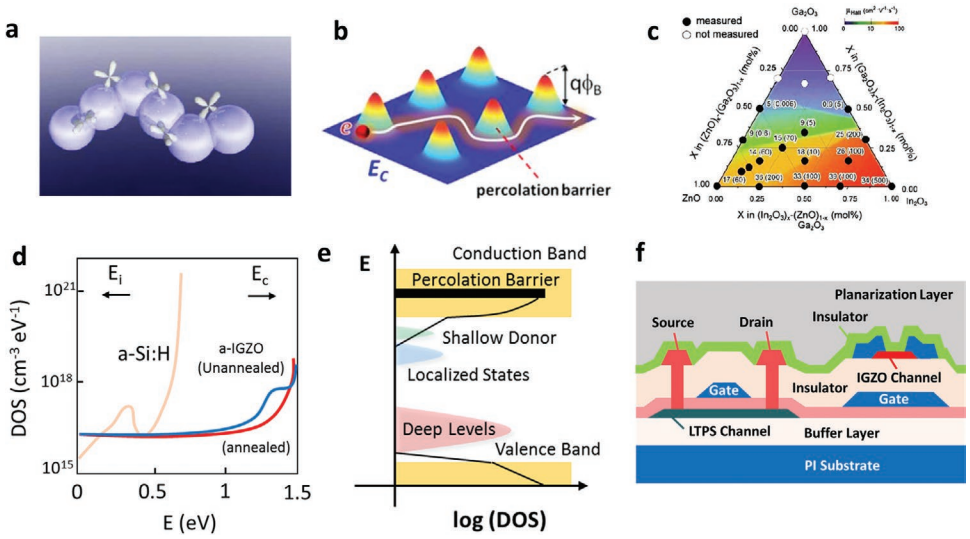

Figure 4. a) Schematic of the orbitals participating in the ionic bonding in a-IGZO. The large overlap of the spherical 5s orbitals of adjacent In atoms is the cause of the high-conductivity despite having an amorphous nature. b) Percolation model in a-IGZO with carriers experiencing statistical (Gaussian) barriers. c) Ternary diagram of the measured Hall μ of a-IGZO with the composition. d) DOS of as-prepared (unannealed) and annealed a-IGZO. DOS of a-Si:H is plotted for comparison. e) Schematic of DOS for a-IGZO with subgap states. f) Hybrid structure of LTPS- and AOS-TFTs (LTPO). a) Reproduced with permission.[52] Copyright 2004, Springer Nature. b) Reproduced with permission.[20b] Copyright 2015, Springer Nature. c) Reproduced with permission.[59] Copyright 2006, Elsevier B.V. d) Reproduced with permission.[61] Copyright 2008, AIP Publishing LLC. e) Reproduced with permission.[64] Copyright 2009, The Optical Society. f) Reproduced with permission.[70] Copyright 2019, Wiley-VCH.

its first applications to AM-OLED in 2006,[55] AOS-based TFTs were adopted in mass-produced AM-LCD in 2012. Nowadays, most of commercial OLED TVs utilize AOS-based TFTs.

4.1.2. Percolation Mechanism for Carrier Transport

Unlike a-Si:H and LTPS, AOS exhibits distinct behavior in the carrier transport. Nomura et al. compared the electrical properties of single-crystalline IGZO (s-IGZO) and polycrystalline IGZO (poly-IGZO) to elucidate conduction mechanism in IGZO.[56] s-IGZO was prepared by 1400 °C annealing of PLD-grown epitaxial $ZnO/InGaO_3(ZnO)_5$ on YSZ (yttria-stabilized zirconia) (111) substrate to undergo solid-phase crystallization of IGZO. poly-IGZO was obtained by direct deposition of IGZO by PLD on YSZ (111).[56,57] The carrier concentration was effectively modulated by H_2 annealing. Then the temperature-dependent μ was obtained by Hall measurements. First, for poly-IGZO, μ showed thermally activated behavior when the carrier concentration $N_e > 10^{19}$ cm^{-3}, and it was almost independent of temperature when $N_e > 10^{18}$ cm^{-3}. The authors interpreted that when $N_e > 10^{18}$ cm^{-3}, E_F is located above CB. However, the carrier transport is limited by GBs since they trap charges and establish potential barrier. As a result, thermally activated behavior is observed.

On the other hand, for s-IGZO, temperature dependency on μ was large when $N_e < 10^{18}$ cm^{-3}, while μ was almost independent when $N_e > 2 \times 10^{18}$ cm^{-3}. At high level of N_e, μ increased significantly with N_e, which implies degenerate conduction. Meanwhile, when $N_e < N_{th}$ ($\approx 3 \times 10^{18}$ cm^{-3}, threshold electron concentration), the conductivity showed $\exp(T^{-1/4})$ (T is a temperature) dependence. Therefore, at low carrier concentration regime, variable range hopping at the localized state is plausible. However, when $N_e > 1 \times 10^{17}$ cm^{-3}, an abrupt increase in conductivity with N_e along with $\exp(T^{-1/4})$ dependence for moderate N_e can only be explained by percolation mechanism. Percolation mechanism is attributed to the potential barriers with Gaussian-type distribution (Figure 4b). If N_e exceed a certain level, E_F becomes located above the percolation barrier and a temperature-independent conduction occurs. Even though IGZO was single-crystalline, the authors suggested that the random distributions of Ga^{3+} and Zn^{2+} in $(GaO)^+(ZnO)_5$ layers be responsible for the modulation of local electronic structure around CB edge and establish statistical potential distribution. Also, for poly-IGZO, the potential barrier by grain boundary is much larger than percolation barrier that results in thermally excited behavior in the conduction of poly-IGZO. Similar to s-IGZO, a-IGZO also follow percolation mechanism in carrier transport.

4.1.3. Role of Constituent Atoms

In the case of AOSs, in general, the carrier concentration is very high. Therefore, the on/off characteristics are not good. Since the carrier originates from O-vacancy, Ga can be added to reduce carrier concentration, and although μ is lowered according to the addition of Ga, I_{off} can be greatly reduced. A density functional theory (DFT) calculation by Noh et al. showed an increase in the formation energy of deep oxygen vacancy increased with the coordination number of Ga, which implies oxygen vacancy formation can be effectively suppressed by Ga addition.[58] On the other hand, when only In_2O_3 is deposited, a crystalline phase is formed spontaneously. However, the addition of cations (Ga, Zn) of a different size from In can form a stable amorphous phase. Figure 4c shows μ of a-IGZO according to the

ratio of In, Zn, and Ga.[59] It can be seen that the μ increases with the ratio of In and Zn but decreases with the ratio of Ga.

4.1.4. Subgap States and the Effect on Annealing

The deposition of IGZO is carried out at low temperature, which inevitably generates defects during the growth process. The DOS for defects are known to be located below the shallow trap of IGZO. Since they are detrimental for the electrical properties, they should be eliminated before device operations. Fortutely, the states can be decreased by simple annealing. Therefore, in general, annealing below crystallization temperature (≈300 °C) is carried out when AOS-TFTs are fabricated.

Nomura et al. evaluated the electrical properties of a-IGZO with the quality of film.[60] The a-IGZO film was prepared by PLD. Depending on the laser energy for target irradiation, the film quality can be changed. That means, low-quality (LQ) samples are produced when using low-power excimer lasers, while high-quality (HQ) samples are produced by high-power lasers. The as-prepared LQ samples had μ of 2.5 $cm^2\ V^{-1}\ s^{-1}$, and it was improved approximately fourfold (≈10 $cm^2\ V^{-1}\ s^{-1}$) when annealed at 400 °C. On the other hand, annealing effect was less significant for HQ samples (μ changed from 15 to 19 $cm^2\ V^{-1}\ s^{-1}$). Meanwhile, hard X-ray photoelectron spectroscopy (XPS) was used to estimate DOS of the film. It showed the subgap DOS of LQ decreased by half by annealing, from 2.6×10^{21} to 1.6×10^{21} cm^{-3}. For HQ film, the subgap state itself is small and it decreased from 9.3×10^{20} to 5.0×10^{20} cm^{-3} upon annealing. Therefore, it can be inferred that the mechanism of annealing-induced μ improvement is largely based on subgap DOS reduction (Figure 4d).[61] Also, due to lowered subgap states by annealing, SS can be improved and operation voltage can become smaller. Meanwhile, the obtained subgap DOS is located at >1 eV deeper than E_F. The large DOS can make Fermi level pinning (FLP) at ≈1.5 eV above VB edge at reverse bias. In this case, subgap DOS is approximately two orders of magnitude larger than the hole concentration that can be induced by applying gate bias. Therefore, they conclude that the p-type conduction is hardly attained in AOSs (DOSs beneath CB is as small as $\approx 10^{18}$ cm^{-3},[62] making electron conduction possible). Also, conduction of holes is highly unlikely, which results in greatly suppressed I_{off} in AOS-based TFTs.

To understand the origin of each subgap state in a-IGZO, Kamiya et al. conducted pseudo-band structure calculation for stoichiometric a-IGZO (sa-IGZO), crystalline IGZO (c-IGZO), and oxygen-deficient a-IGZO (oa-IGZO).[63] Interestingly, sa-IGZO had no subgap states, which was also observed in the case of c-IGZO. The dispersion in the CB was very large (also effective mass for electron is small) in both sa-IGZO and c-IGZO, implying the transport of electrons are not highly affected by the order of IGZO. However, for VB, dispersion was very small for sa-IGZO while it was little small for c-IGZO. This indicates that a break in the covalent hybridization of directional O 2p orbitals in sa-IGZO results in strong localization of VB, which is constituted mainly of O 2p orbitals. For oa-IGZO, deep and fully occupied (V_O^0) states were found to locate at 0.4–1 eV above VB edge (deep donor state at Figure 4e).[64] Also, oa-IGZO showed large reduction in dispersion of the lowest unoccupied bands at ≈0.6 eV compared to sa-IGZO. This implies that the formation of V_O^0 may break the coherency in CB edge, and possibly make small but localized state near CB edge (shallow donor state at Figure 4e).

4.2. Novel Device Structures

4.2.1. Doping Method for Amorphous Oxide Semiconductors

Unlike a-Si:H or LTPS, highly doping AOSs by incorporating impurity atoms is not well established and hard to be achieved. It is due to ionic nature of AOSs that the addition or elimination of electrons may not contribute to the change in formal charge. That might be a reason for the commercial AOS-based TFTs adopt both bottom-gate, staggered structure and top-gate, self-aligned structures. Indeed, the doping is possible by a simple plasma treatment. Park et al. fabricated a bottom-gate staggered structure using a-IGZO as an active layer.[65] Whole surface of the as-deposited a-IGZO was treated by Ar plasma, and after that source and drain electrode were deposited. After plasma treatment, the carrier concentration increased from 10^{14} to 10^{20}–10^{21} cm^{-3}, and the field effect mobility (μ_{FE}) increased from 3.3 to 9.1 $cm^2\ V^{-1}\ s^{-1}$. They then annealed the samples in air and measured the resistivity. However, they found that resistivity increased more than three orders of magnitude while the composition of cations detected by XPS was not changed. Therefore, they proposed that energetic Ar ion during plasma treatment would preferentially sputter oxygen atoms in a-IGZO. This makes oxygen deficiencies in a-IGZO, which could contribute to an increase the carrier concentration.

Park et al. evaluated the performance of a-IGZO TFTs using highly doped a-IGZO as an ohmic contact layer.[66] Top-gate, coplanar and self-aligned TFTs were fabricated and the a-IGZO layer that contact with source and drain electrode was selectively exposed to Ar plasma. The extracted μ_{FE} was 5 $cm^2\ V^{-1}\ s^{-1}$. To elucidate the mechanism of doping, the authors analyzed secondary ion mass spectroscopy (SIMS) and Rutherford backscattering spectroscopy (RBS). From SIMS analysis, contrary to previous reports by Park et al.,[65] the oxygen concentration among various samples were similar, which implies In–O bond is just broken and results in segregation of In on the surface. RBS analysis also confirms that the composition was changed up to ≈6 nm in depth. For sheet resistance measurements, regions up to ≈40 nm in depth were affected by plasma treatment.

Ahn et al. fabricated bottom-gate, self-aligned a-IGZO TFTs. They compared the effect of Ar and H_2 plasma treatment on the contact region of active layer with source and drain electrodes. When plasma was treated, the carrier concentration dramatically increased from 10^{14} cm^{-3} to 9.5×10^{19} cm^{-3} and 1.5×10^{20} cm^{-3} for Ar and H_2 plasma treated samples, respectively. From SIMS profile of H and OH, they found that the concentration of H and OH also significantly increased up to ≈50 nm depth. This can be explained by diffusion of H, not by sputtering of O atoms by H since momentum transfer by light H atoms during plasma treatment is very low. Thus, H atoms may act as a shallow donor. Therefore, unlike Ar plasma treatment

that affects only up to shallow depth (≈5 nm), H_2 plasma treatment was more effective to decrease R_c (128 and 75 Ω cm for Ar and H_2 plasma treated samples, respectively) and increase μ_{FE} (4.27 and 7.27 $cm^2\ V^{-1}\ s^{-1}$ for Ar and H_2 plasma treated samples, respectively). If plasma treatment or UV treatment is not performed, the Schottky barrier can be formed and that lead to an increase in R_c. Extraction of specific R_c showed linear relationship between R_c and φ of electrode materials (i.e., smaller φ of electrodes results in smaller R_c).[67] In that case, for Ti, possible formation of oxidized interfacial layer may lead to a broad range of R_c.

Meanwhile, since AOSs are transparent, it is possible to fabricate fully self-aligned double-gate TFTs by UV exposure (transmittance over 70% at 365 nm) from the back side to pattern top-gate.[68] The double-gate structure shows improved bias stability and enhanced carrier μ than single-gate structures. With the Ar plasma treatment for the contact region and injection of H atoms by PECVD-SiN_x passivation, He et al. extracted saturation μ of 11.3, 9, and 4.2 $cm^2\ V^{-1}\ s^{-1}$ for double-gate, top-gate, and bottom-gate structures, respectively, and explained that the enhanced μ is attributed to reduced roughness scattering by lowered vertical electric field. Practically, SiN_x as GI is not favored because of small band gap-induced large bias instability and not good interface properties.

4.2.2. Low-Temperature Polysilicon Oxide

Recently, low-temperature polysilicon oxide (LTPO) was emerged as a platform for high-end displays demanding low power consumptions (e.g., smart watch, smart phone) and applied in commercial products.[69] LTPO is not new materials, but the combination of LTPS and AOS technology. Typically, LTPO consists of LTPS-TFT backplane for peripheral circuit and driving TFTs, and embedded AOS TFTs for switching TFTs (Figure 4f).[70] Therefore, low-frequency driving is possible due to very low leakage current of AOS-TFT, while the power consumption can be low by high μ LTPS and low-frequency driving scheme. Also, the peripheral circuit size can become smaller by LTPS, which is advantageous for slim bezels. One of the key issues to be solved for the realization of LTPO is the control of hydrogen diffusion. Plenty of hydrogen is used to passivate defects at grain and within grain boundaries. However, they can make bond with AOS and change DOS originated from oxygen vacancies. This ultimately can shift V_{th} of AOSs, emphasizing the importance of hydrogen concentration control during LTPS processes.[71]

4.3. Bias Stress Instability

Like a-Si:H, AOSs are sensitive to the bias stress conditions. An initial work by Suresh et al. showed that the ΔV_{th} with the stress time is parallel without change in SS or μ_{FE}.[72] As mentioned in Section 2.3, this is typically observed in a-Si:H when charge trapping is more dominant than defect creations. When positive bias is applied, V_{th} was moved toward the positive direction with time, indicating electrons are trapped at the interface between channel and GI or the electrons are injected to GI. Applying negative bias did not show any effects since all the carriers in the channel were depleted. In terms of ΔV_{th} value with the growth condition, a-IGZO deposited at high O_2 pressure showed low ΔV_{th} since the intrinsic concentration of carriers (from oxygen vacancy) was low. Similar result was also reported by Ji et al.[73] They tested various samples of a-IGZO post-annealed at different O_2 pressures under negative bias illumination stress (NBIS). Unlike negative stress test in dark conditions, light illumination excites oxygen vacancies and generate free carriers, and this largely shifts ΔV_{th} in a negative direction. When oxygen pressure was high (or low oxygen vacancy concentration), ΔV_{th} to the negative direction was small. Therefore, the authors proposed that photo-induced transition of oxygen vacancy (from V_O to V_O^{2+}) is responsible for NBIS instability. Nomura et al. evaluated ΔV_{th} for the as-deposited, post-annealed at 400 °C in both dry and wet O_2 atmosphere. When the thermal decomposition spectra were measured, unannealed samples showed a large increase in shallow traps due to metastable bonds which easily desorb under stress conditions (Zn-O, H, OH-related species). They suggested that the annealing greatly suppress this phenomenon and make the samples less susceptible to the bias stress.

Similar to a-Si:H, stretched-exponential models are widely used to interpret bias instability in AOSs. Lee et al. showed that the conventional logarithmic model of ΔV_{th} that is derived solely from charge trapping mechanism may not agree well with the experimental data in AOSs.[31] As mentioned earlier, logarithmic time dependence model assumes no redistribution of trapped charges in GI, suggesting stretched-exponential models may fit better to the AOSs.

5. Transition Metal Dichalcogenides TFTs

5.1. Growth Strategy of TMDCs for Display TFT Applications

5.1.1. Low-Temperature Growth of TMDCs

The deposition temperature of a TFT channel material is limited by the temperature that the substrate can withstand. Although the composition of the substrate is tunable to enhance thermal stability, a commercially available substrate is designed to endure up to ≈600 °C due to cost issues. However, the process temperature of common growth methods as thermal CVD is typically beyond the limit, which is 700–1100 °C (**Figure 5**a,b).[74] Since lowering the growth temperature has a trade-off in the film quality and growth speed, special actions have to be taken to grow high-quality films with reduced thermal energy: 1) grow at low pressures, 2) shift an equilibrium using Le Chatelier's principles, 3) utilize nucleation promoters, 4) reduce an activation energy for a reaction, and 5) enhance the surface diffusion rate.

The first strategy is based on the deposition limited by mass transport of chemical species at moderately reduced pressures, where the mass transfer coefficient is inversely proportional to the square root of pressure. Under this strategy, Mun et al. reported MoS_2 with a grain size of 100–200 nm grown for 8 h at 250 °C and a moderate pressure of 30 torr. Here, the growth temperature is more than 250 °C lower than that of

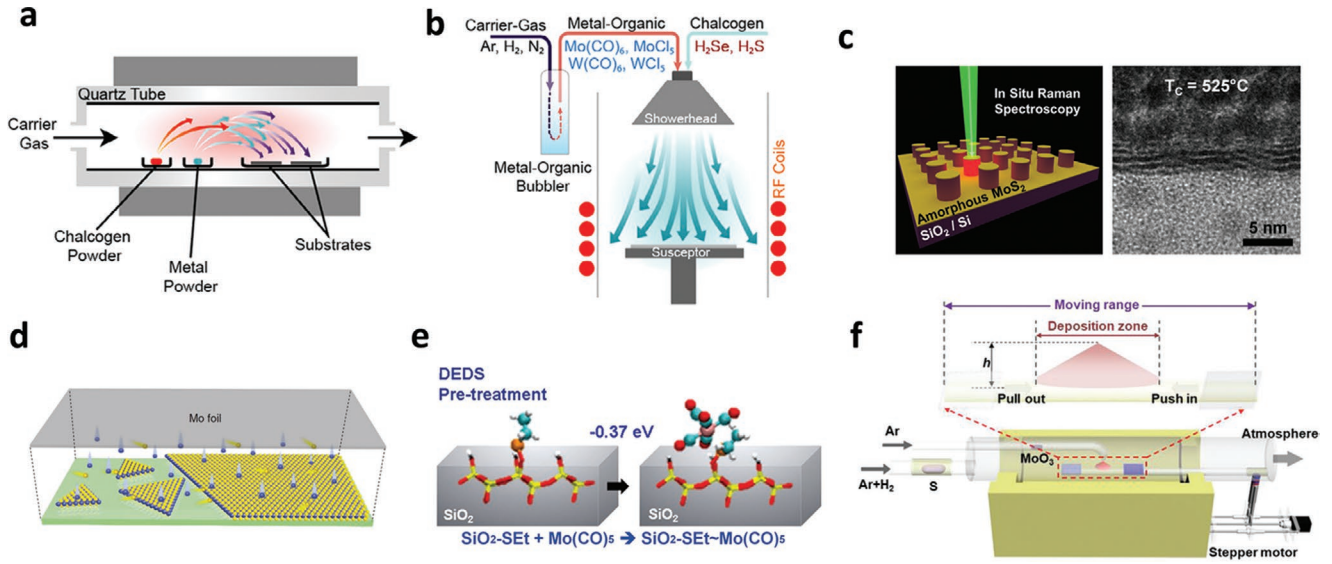

Figure 5. a,b) Schematic of the typical growth system of TMDCs. a) CVD and b) MOCVD. c) Schematic of the laser-crystallization of sputter-deposited amorphous MoS_2 into crystalline MoS_2 and the corresponding cross-sectional TEM image. d) Face-to-face growth strategy for large-area uniform growth. e) Schematic showing that the chemisorption of a precursor molecule ($Mo(CO)_6$) is inhibited by the steric hindrance of an inhibitor (DEDS)-treated surface, leading to a controlled growth of MoS_2 by iALD. f) Uniform growth strategy of moving substrates to maintain constant growth conditions. a,b) Reproduced with permission.[74] Copyright 2019, IOP Publishing. c) Reproduced with permission.[84] Copyright 2018, IOP Publishing. d) Reproduced with permission.[90b] Copyright 2018, Springer Nature. e) Reproduced with permission.[92] Copyright 2017, Wiley-VCH. f) Reproduced with permission.[96] Copyright 2019, IOP Publishing.

typical CVD (>500 °C).[75] The second strategy is based on the fact that the chemical reaction proceeds in a direction maintaining its equilibrium. That is, the forward reaction is likely to occur if the concentration of the reactants becomes higher. Therefore, increasing the concentration of reactants during the deposition will assist the formation of MoS_2. When using a solid precursor, this can be achieved by lowering the pressure to promote its evaporation (droplet evaporation theory[76]), thereby increasing the partial pressure. Alternatively, it can be done by using large amounts of precursors or easily decomposable precursors at low temperatures (i.e., having high vapor pressures). Through this approach, Ji et al. reported the growth of MoS_2 with a crystallinity of ≈1 µm when grown for 30–60 min at 530 °C and 0.23 torr using typical precursors for CVD-MoS_2 (MoO_3 and sulfur).[77] In the case of the third strategy, when aromatic molecules are added, they evaporate and condensate to form heterogeneous nuclei. This lowers the barrier to nucleation and can promote low-temperature growth.[78] In the fourth case, since the reaction rate constant is proportional to exp $(-E_a/kT)$ (where E_a is the activation energy for the reaction), lowering E_a by adjusting the reaction path can lower the growth temperature. For example, in a study by Gong et al., the growth of MoS_2 with a crystallinity of over 100 µm at 450 °C is shown when $(NH_4)_2MoO_4$ is used as a precursor.[79] The decrease in E_a was demonstrated through a DFT calculation. Similarly, growth assisted by Au catalysts or alkali metal halide catalysts can be classified into such examples.[80] Thermogravimetry and differential scanning calorimetry (TG-DSC) measurements indicate that the mixing of alkali metal halides with metal oxides pushes the melting point of most transition metal oxides to within the range of 600–800 °C.[80b] In this way, all TMDCs on the periodic table can be grown within this temperature range, although alkali metals that are introduced during the reaction have a significantly bad effect on the reliability of the device, and thus have limitations in their actual application. The fifth strategy can be achieved by utilizing a liquid substrate that can take advantage of the rapid movement of atoms adsorbed on the surface. Zhou et al. reported the synthesis of crystalline 2D GaSe and 2D $Ga_xIn_{1-x}Se$ at low temperatures of 100–150 °C using Ga and In-Ga alloys with a melting point of ≈30 °C.[81] Wang et al. was able to synthesize tens of micrometer-sized $Ga_2In_4S_9$ ternary alloys at low temperatures of 300–450 °C by heating the In-Ga alloy (In:Ga = 1:3) at 950 °C and supplying sulfur.[82] Here, small binding energy between Ga or In and a chalcogen atom may also contribute to lower the growth temperature. Similarly, when Te (melting point of 450 °C) is mixed with W (melting point of 3422 °C), W is dissolved in Te at 450 °C and forms an alloy with W, thus synthesizing WS_2 at a low temperature of 500 °C becomes possible.[54] Despite the relatively low growth temperature, highly crystalline (≈50 µm) MoS_2 was obtained.

Meanwhile, similar to the growth of a-Si:H, the growth of a-MoS_2 can be achieved at a low temperature using PECVD. Ahn et al. prepared a 4 inch PI substrate with 1 nm (five to six layers) of Mo deposited using an electron beam evaporator.[83] When plasma is formed, the injected H_2S molecules collide with Ar^+ ions, forming H_2S^+ ions. These H_2S^+ ions can then be accelerated in the sheath region located near the growth substrate. The accelerated ions can collide with Mo, and finally a MoS_2 film is created. The thickness of the film was measured as 3–4 nm (five to six layers); however, the domain size of the film grown at 150 and 300 °C was 5 and 7 nm, respectively. This implies that, similar to a-Si, a uniform film can be

obtained over a large-area using PECVD, although the quality of MoS_2 has a certain limitation.

As in the case of LTPS, it is clear that the crystallization of as-grown a-MoS_2 using a laser can improve the quality of the a-MoS_2. This approach was applied by Vilá et al. (Figure 5c).[84] Under high vacuum conditions, a diode-pumped continuous wave laser (532 nm) was continuously focused on the sputtered a-MoS_2 on a SiO_2/Si micro-pillar to heat the overall substrate, which subsequently annealed the entire a-MoS_2 film through heat conduction. The a-MoS_2 underwent a solid-state phase transformation during isothermal heating, resulting in crystallized 2H-MoS_2. By monitoring the reference Si peak shift from room temperature, the crystallization temperature of a-MoS_2 can be inferred. The integrated Raman peak intensity of $E_{2g}{}^1$ and A_{1g} over time can then provide information on crystallization kinetics. From an Arrhenius plot for a rate constant, the energy barrier for crystallization was estimated to be 1.03 eV per atom, which implies that sulfur diffusion (1.04 eV per atom for diffusion in MoS_2 as predicted through DFT calculations) may play a crucial role in crystallization.

Along with laser sources, xenon flash lamps with a broad light spectrum have also been spotlighted as a scalable and cost-effective tool for a novel light-material interaction owing to their large-area processability and excellent compatibility to the roll-to-roll process.[85] Kim et al. employed a large-scale (>6.25 cm^2) intensely pulsed light source to induce a controlled photonic crystallization of an a-MoS_2 film.[86] The a-MoS_2 sputtered on polydimethylsiloxane (PDMS) was treated through a flash lamp process in air, leading to a phase transformation into 2H-MoS_2 without a decomposition of the polymer substrate. However, flash-induced MoS_2 heating upon crystallization causes a mismatch of the thermal expansion coefficient between the MoS_2 and PDMS, which results in a uniform wrinkling of the MoS_2/polymer.

5.1.2. Uniform and Scalable Growth of TMDCs

Typically, thin film deposition in the semiconductor process takes place at low pressure. This is because not a mass-transport-limited growth but a surface-reaction-limited growth occurs at low pressure, thus enabling highly uniform and conformal growth of thin films. Therefore, for the purpose of uniformity in TMDC growth, low-pressure CVD has been widely used. Transport phenomena simulations also support that the growth at low pressure is more advantageous in uniformity than high pressure in the layered material growth.[87] To date, low-pressure growth has been reported to enable growth of up to 4 inch (7.5 torr) and 6 inch (20 torr) wafers in metal-organic CVD (MOCVD) and CVD.[88] Also, uniformly coating the precursor on the surface can achieve a large-area, uniform growth. By means of reacting predeposited WO_x film under Se atmosphere, growth of up to 8 inch wafers (1–10 torr) has been reported.[89] Alternatively, disposing uniformly coated (or deposited) precursor substrates facing the growth substrate can be used. This approach is similar to the use of multiple rotating cylindrical target arrays to form uniform films for the large-area deposition of a-IGZO.[53] Using this method, uniform growth up to 1.5 × 3 cm^2 at the atmospheric pressure (760 torr) and up to 6 × 14 cm^2 at low pressure has been reported (Figure 5d).[90] Self-limited reactions can also be used to form uniform thin films. When annealed after coating a mixed solution of $(NH_4)_2MoO_4$ and KOH on the surface, the migration of -OH groups to the MoS_2 (001) surface became thermodynamically stable, resulting in a uniform thin film without ad-layers.[91] In addition, when Au foil is used as a substrate, an atomically thin layer is obtained through the low solubility of Mo or W to Au. Ad-layer growth rate on the as-grown MoS_2 or WS_2 is very low, which results in a strictly monolayer.[80a] Using methods based on self-limiting growth mechanisms (atomic layer deposition or ALD, inhibitor-utilizing ALD or iALD) yield uniform films regardless of the substrate size (Figure 5e), and up to a 6 inch wafer level growth has been reported.[92] Although a suitable method on a lab-scale, molecular beam epitaxy (MBE) is also possible for the growth of a uniform thin film, which is currently reported up to 2 inches.[93]

5.1.3. Thickness-controlled Growth of TMDCs

The electrical properties of TMDCs are highly sensitive to the thickness due to the atomically thin nature. In the case of a thick layer, μ decreases by a low interlayer conductivity, while for thin layers, lowering in μ is attributed to the scattering by influence from the interface.[94] Therefore, thickness-controlled growth is essential to modulate the electrical properties. However, the possibility of the layer-controlled growth depends on the physical properties of the TMDCs. There are two governing processes for the growth: one is nucleation and the other is the growth itself. If the growth rate is dominant, the number of layers is limited because a small and thin nucleus is formed.[80b] If the ripening rate during the nucleation process is dominant, multilayer growth is preferred owing to the large nuclei formed. This may explain the layer number tendency of CVD-MoX_2 (X = S, Se, Te) that is typically observed. Since sulfur has a higher vapor pressure than Se and Te at the same temperature, the growth of MoS_2 occurs faster than $MoSe_2$ and $MoTe_2$. As a result, monolayer growth is preferred for MoS_2, while multilayer growth is frequently observed for $MoTe_2$. Therefore, the type of TMDC should be carefully chosen to control the number of layers.

Meanwhile, layer-controlled growth is possible even if the layered growth might be not preferred for certain TMDCs. However, there is a trade-off between the thickness and the quality of the film. Taking MoS_2 as an example, because the surface energy of the edge is ≈130 times larger than the basal plane,[95] after one layer is grown on the substrate, the next layer becomes difficult to grow due to a change in the surface energy of the growth substrate. Therefore, the as-grown layer must be defective to allow nucleation and multilayer growth to occur.[96] This process is achieved at the expense of the film quality. In addition, nuclei formation during the growth process is achieved by either seed-mediation (PTAS, etc.) or self-seeding by a cluster or core-shell formation.[97] During this process, however, a 10–20 nm sized seed is inevitably formed, and even though it looks flat and uniform when observed through optical microscopy, its impact on the electrical characteristics can be

detrimental.[98] Therefore, meeting high-quality and layer-controlled growth at the same time is extremely challenging.

Various methods have been proposed for layer control in sulfide compounds, which are relatively disadvantageous for layered growth. Jeon et al. reported that the thickness of the MoS_2 can be controlled in mono-, bi-, and tri-layers by increasing the interaction of the MoS_2 precursor with the substrate through O_2 plasma treatment of the substrate surface.[99] Song et al. obtained mono-, bi-, and tri-layer WS_2 through the sulfurization of plasma-enhanced ALD-deposited WO_3 with H_2S.[100] Lee et al. obtained 2, 4, 8, and 12 layers of MoS_2 when a thick Mo thin film was deposited and sulfurized with H_2S.[101] However, the grain size measured by high-resolution transmission electron microscopy (HRTEM) was extremely small (10–20 nm). In a precursor deposition-based method, volume expansion occurs owing to a deformation of the lattice structure during sulfurization. When the thickness of Mo film exceeds 3 nm, vertical growth occurs and thereby releasing the strain.[102] Zafar et al. reported that increasing the feeding rate of sulfur promotes the formation of a large WO_xS_{2-y} clusters in the gas phase, increasing the number of layers of WS_2 up to four.[103] He et al. reported that the thickness of MoS_2 can be controlled from a monolayer to up to 30 layers by periodically inserting and removing the substrate using a motor and modulating the number of cycles (Figure 5f).[96] This method has an advantage of forming a uniform thin film (1.5×1.5 and 0.6×4.7 cm^2) in the lateral direction because it is exposed to a uniform growth environment. However, a non-uniformity of the crystal size was observed in the direction perpendicular to the substrate. The grain size of the first layer was several micrometers, but the grain size decreased as the number of layers increased.

5.2. Mobility Engineering Strategy of TMDCs for TFT Applications

5.2.1. Generalized Mobility Model for TMDCs

μ refers to the ability of a charge carrier to drift in the direction of an electric field when an electric field is applied. Based on a formula, μ represents the ratio of the applied electric field to the average drift velocity, which is mainly affected by a scattering from the Coulomb interactions among the charged impurities in a lattice and charge carriers, and also from the thermal vibrations in the lattice. Here, lattice vibration from thermal energy is periodic and can be described as quantized particles, which are called phonons. The phonon mode is divided into an optical mode, in which adjacent atoms move in the opposite direction, and an acoustic mode, in which adjacent atoms move in the same direction. According to the directions of the vibration and wave propagation, they are divided into longitudinal (parallel) and transverse waves (perpendicular). Meanwhile, if we consider a model where atoms are connected by springs, in optical mode the spring is stretched more than in acoustic mode, resulting in a higher elastic potential energy. Therefore, when the temperature is low, the scattering by the acoustic phonons predominantly occurs, and when the temperature is high, excitation of the optical phonons contributes largely to the scattering.

So far, numerous models have been proposed to predict the intrinsic μ in bulk semiconductors. A similar approach can be used for the atomically thin 2D materials, however, μ must be newly assessed because the band structure changes as the scale decreases to nanometer level and the contribution of the surface properties increases. Kaasbjerg et al. theoretically predicted the phonon-limited μ in a single-layer MoS_2.[104] In this case, at low temperature regime (e.g., 100 K), μ is predicted to be $\mu \approx T^{-\gamma}$ where $\gamma = 1$ because the influence of the longitudinal acoustic (LA) and transverse acoustic (TA) phonons is important at low temperatures. As the temperature increases, the transverse optical (TO) phonons, the homopolar phonons (HPs), and the Fröhlich scattering (scattering by the longitudinal optical phonons) become stronger, and thus γ is predicted to be 1.69 at room temperature. For reference, γ is known to be ≈2.6 in a bulk material. Meanwhile, according to Matthiessen's rule, μ can be expressed as the sum of the reciprocal of μ by each contributing mechanism because μ is proportional to the scattering rate of the charge carriers (**Figure 6**a).[105] As a result, μ of a single-layer MoS_2 at room temperature was estimated to be 410 $cm^2\ V^{-1}\ s^{-1}$ when considering five phonon scattering mechanisms. Radisavljevic et al. used a double-gate structure to improve μ significantly (≈200 $cm^2\ V^{-1}\ s^{-1}$) compared to previous reports.[106] In this structure, the homopolar mode (out-of-plane vibrational mode) is quenched.[104] When the contribution of the homopolar mode was excluded, the estimated μ was ≈70 $cm^2\ V^{-1}\ s^{-1}$. Therefore, impurity screening from the deposition of a high dielectric constant (κ) GI was expected to contribute significantly to the increase in the experimental μ. In addition, for the scattering caused by impurities to prevail, the distance between the impurities must be on the same order or smaller as the mean free path of the phonons. This corresponds to the minimum impurity concentration of $\approx 5 \times 10^{11}$ cm^{-2}. As a result of this strong doping, the authors suggested that the typical mechanically exfoliated MoS_2 has a low μ.

When a high-κ GI such as HfO_2 is used, surface optical (SO) phonon (or remote polar phonon) scattering occurs. This scattering is induced by the optical phonon mode of the thin film with a high-κ, in which oscillating dipoles are formed. At this time, because the electric field induced from the dipole is an evanescent field that cannot propagate to a large distance, the electric field is exponentially reduced with the distances, and thus its influence is limited near the interface of a high-κ GI. Therefore, in Si-based devices, SO phonons are typically influential when an inversion layer is formed. Meanwhile, TMDCs are largely affected by SO phonon scattering due to their atomically thin nature. To evaluate this, Ma et al. predicted μ when MoS_2 was in contact with several different dielectrics.[107] At this time, a single layer of MoS_2 was assumed to be surrounded by an insulating film of infinite thickness, and thus the effect of the dielectric was slightly overestimated. Assuming that a charge has formed from an impurity in the MoS_2, when a high-κ GI is used, the electric field from the charge is screened to reduce the carrier scattering by the impurity. In addition, a screening effect was observed when the concentration of free carriers was high. On the other hand, as κ value of GI increases, the angular frequency of the SO phonon (ω_{SO}) decreases, which increases the SO phonon scattering effect. This scattering effect is negligible at low temperature ($T < 100$ K) because the SO phonons

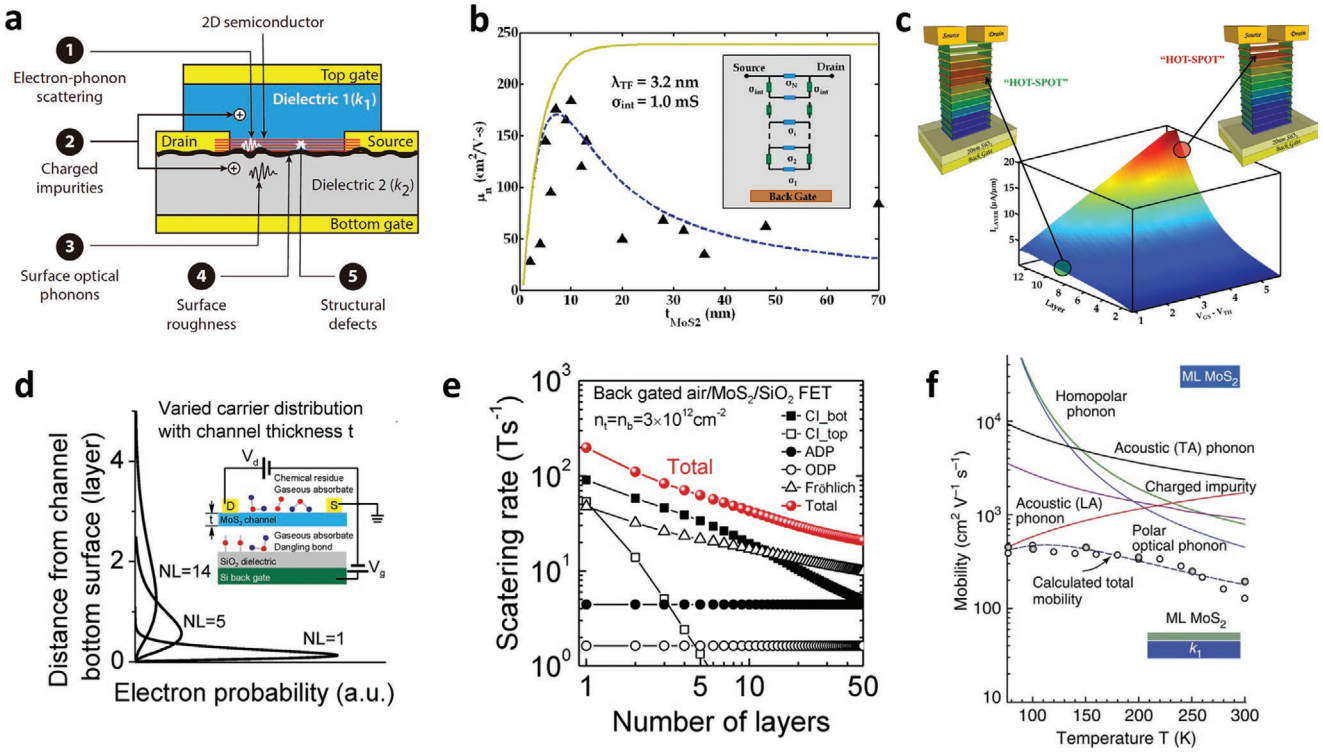

Figure 6. a) A typical dual-gate TFT using 2D materials as the channel, showing various origins of charge scattering. b) Resistor network model for a multilayer MoS_2 TFT without (yellow solid line) and with (blue dotted line) interlayer resistance. c) Simulated distribution of current flow with the applied voltages in multilayer MoS_2. d) Lopsided carrier concentration distribution model of MoS_2 with the number of layers. e) Calculated scattering rate of μ from each scattering source in a MoS_2 TFT. f) Contribution of several scattering sources to μ of multilayer MoS_2 with temperature. a) Reproduced with permission.[105] Copyright 2018, Annual Reviews. b–e) Reproduced with permission.[94,112a,114] Copyright 2013, American Chemical Society. f) Reproduced with permission.[115] Copyright 2012, Springer Nature.

are not populated at low temperatures, but are dominant over impurity scattering at room temperature. For example, if no SO phonon scattering occurs in the $SiO_2/MoS_2/HfO_2$ structure, μ is expected to be ≈130 (when $N_I = 6 \times 10^{12}$ cm^{-2}, $n_s = 1.15 \times 10^{13}$ cm^{-2}) and ≈1400 cm^2 V^{-1} s^{-1} (when $N_I = 2 \times 10^{12}$ cm^{-2}, $n_s = 1 \times 10^{13}$ cm^{-2}). However, when SO phonon scattering is present, μ is reduced to ≈50 and ≈70 cm^2 V^{-1} s^{-1}, respectively. Here, N_I is the concentration of impurities, and n_s is the concentration of free carriers in MoS_2. In this case, when only SO phonon scattering is considered, μ is ≈70 cm^2 V^{-1} s^{-1}. However, μ_{ph}, which considers the intrinsic phonon-limited μ and SO phonon scattering, decreases as κ increases. For extreme conditions of air/MoS_2/air or free-standing MoS_2, the value of μ_{ph} can be improved to ≈10 000 cm^2 V^{-1} s^{-1}. By contrast, when the concentration of impurities is high (>10^{12} cm^{-2}), an impurity scattering becomes μ-limiting factor and thus dielectrics are barely influential to μ. Therefore, the authors suggested that the samples be clean and have a low concentration of impurities and a GI with a moderate κ value (e.g., h-BN are AlN) to achieve high μ.

Meanwhile, the more polarizable the M-O bond becomes, the larger the SO phonon scattering and the smaller ω_{SO} becomes. Because EN difference between the two elements determines the ionic characteristic of the bond, EN of the elements can provide a guideline for finding a GI suitable for TMDC materials. For example, in the case of an oxide, considering Pauling EN, SiO_2 ($\Delta EN_{Si,O}$ = 1.54) has a ω_{SO}^1 of 55.6, whereas Al_2O_3 ($\Delta EN_{Al,O}$ = 1.83) has a ω_{SO}^1 of 48.18, ZrO_2 ($\Delta EN_{Zr,O}$ = 2.11) has a ω_{SO}^1 of 16.67, and HfO_2 ($\Delta EN_{Hf,O}$ = 2.14) has a ω_{SO}^1 of 12.4. For nitride, BN ($\Delta EN_{B,N}$ = 1.00) has a ω_{SO}^1 of 93.07, whereas AlN ($\Delta EN_{Al,N}$ = 1.43) has a ω_{SO}^1 of 81.4.[51,107] Here, assuming a spring model, the angular frequency ω between two atoms is proportional to $(1/m_A + 1/m_B)^{-0.5}$ (where m_A and m_B are the atomic weight of atoms A and B, respectively), and thus the smaller the atomic weight, the higher ω_{SO} can be.

The above results suggest that a multilayer GI can be effective in improving μ characteristics when compared to a single layer GI. Li et al. reported that μ can be increased through the use of a stack structure of GI.[108] To compare the electrical characteristics with GI, a dual-gate device using 4.2 nm thick MoS_2 as a channel was fabricated. SiO_2 was used as the bottom-gate GI and Al_2O_3/HfO_2 was used as the top-gate GI. μ measured at 300 K was 55 cm^2 V^{-1} s^{-1} with the SiO_2 insulating film, but increased to 81 cm^2 V^{-1} s^{-1} with Al_2O_3/HfO_2. The enhanced μ is due to a dielectric screening effect when using a high-κ GI, while good interfacial properties of Al_2O_3 with MoS_2 (as compared to those of SiO_2) are satisfied at the same time. In fact, low-frequency $1/f$ noise measurement indicated that the noise amplitude was reduced by more than 40% in the device with Al_2O_3/HfO_2 GI, and the extracted trap density was reduced by approximately twofold. Similarly, Yu et al. reported that μ_{FE} of a single-layer MoS_2 at room temperature can be increased to 148 cm^2 V^{-1} s^{-1}

using high-κ oxide (10 nm)/SiO_2 (285 nm) multilayer GI.[109] The increase in μ was mainly due to the suppression of the CI scattering by using high-κ GIs. As the κ value increased while CI density remains constant, μ increased in order of SiO_2 (81 $cm^2\ V^{-1}\ s^{-1}$), Al_2O_3 (113 $cm^2\ V^{-1}\ s^{-1}$), and HfO_2 (148 $cm^2\ V^{-1}\ s^{-1}$). Here, μ_{FE} can also be improved by controlling the carrier density by gate voltage.

Meanwhile, point defects (e.g., a vacancy) and line defects (grain boundaries) are present in TMDCs. Majority of them are sulfur vacancy, which is known to contribute to CI scattering and short-range scattering. Yu et al. reported that μ_{FE} can be improved by inhibiting the scattering at the vacancies through a passivation of the sulfur vacancy.[110] In this case, (3-mercaptopropyl)trimethoxysilane (MPS) was used for passivation of the sulfur vacancy. When MPS reacted with a single layer MoS_2 and subsequent annealing is carried out, the sulfur vacancy was replaced with sulfur. From HRTEM images, the density of the sulfur vacancy was found to decrease from $\approx 6.5 \times 10^{13}$ to $\approx 1.6 \times 10^{13}\ cm^{-2}$, which reduces the CI scattering. Reduction in trap density also led to a decrease in the short-range scattering rate, then μ increased by approximately threefold, from 26 to 81 $cm^2\ V^{-1}\ s^{-1}$. Lin et al. reported five defects, namely, V_{Se} (selenium vacancy), Se_W (tungsten vacancy substituted by W), V_W (W vacancy), impurities (e.g., Fe, Mo, and Au emitted from a stainless susceptor or quartz tube during the growth), and Se interstitials when measuring scanning tunneling microscopy (STM) images at 5 K in MOCVD-WSe_2.[111] Scanning tunneling spectroscopy (STS) showed that V_{Se}, Se_W, and V_W form mid-gap states within the band gap, whereas impurities and Se interstitials do not form mid-gap states, and do not affect the electrical properties. When the as-grown WSe_2 was annealed at 850 °C under H_2Se atmosphere, V_{Se} and Se_W decreased by approximately tenfold, and V_W was mostly eliminated. As a result, 800 °C grown WSe_2 with reduced defects showed μ_{FE} of 29.4 $cm^2\ V^{-1}\ s^{-1}$, whereas 650 °C grown WSe_2 with high defect density showed much lower μ_{FE} of 0.083 $cm^2\ V^{-1}\ s^{-1}$.

5.2.2. Effect of Thickness on the Mobility of TMDCs

In general, μ of an atomically thin TMDC is much lower than a bulk material. Das et al. insisted that this phenomenon is in part due to the Schottky barrier between the metal and TMDC material, but mostly affected by scattering from a charged impurity (CI), the contribution of the non-uniform distribution of charges due to charge screening, and the contribution of the interlayer resistance.[94,112] To explain this, a resistor network model was introduced. According to this model, in the case of a bottom-gate device, when the gate voltage is applied, charges are accumulated in the GI. The charge accumulated in the GI becomes $C_{ox}(V_{gs}-V_{th})$, in which image charges are induced in the MoS_2 layer. If there is no screening effect, the charges are evenly distributed in MoS_2. If a screening is present, the electric field applied to the charges on the far side from the gate is screened by the charges gathering on the near side, and the amount of charge induced decreases away from the gate. By contrast, the source and drain electrodes are located at the top, which is directly connected to the top MoS_2 layer. To access the bottom MoS_2 layer, the interlayer resistances (R_{int}) caused by the van der Waals (vdW) gap must be overcome (Figure 6b). In addition, resistance occurs even when electrons flow in MoS_2 laterally, and thus the flow of electrons can be described through the network connection. Because scattering by CI also affected by a screening effect, the scattering effect decreases as it moves away from the bottom-gate (i.e., as it is nearer to the source and drain). That is, μ in the i-th layer from the bottom-gate can be expressed as Equations (3) and (4).

$$\frac{Q_i}{Q_{i-1}} \approx \exp\left(-\frac{d_{ML}}{\lambda}\right) \tag{3}$$

$$\mu_i = \mu_1 + (\mu_\infty - \mu_1)\left(1 - \exp\left(-\frac{(i-1)d_{ML}}{\lambda}\right)\right) \tag{4}$$

where Q_i is the charge induced in the i-th layer, μ_1 is the μ in the first layer, μ_∞ is the maximum μ when there is no scattering effect, d_{ML} is the thickness of a single layer, and λ is the Thomas-Fermi screening length.

For a 13-layer MoS_2 TFT with Sc as source and drain electrodes, Sc has a low φ and thus R_c owing to Schottky barrier height (SBH) of 30 meV was estimated as 0.65 kΩ μm. However, the measured R_c was much larger than this. This indicates that mechanisms other than SBH contribute to the R_c. When fitted using a resistive network model, values of d_{ML} = 0.6 nm, λ = 7 nm, R_{int} = 2400 Ω μm, μ_1 = 30 $cm^2\ V^{-1}\ s^{-1}$, and μ_∞ = 800 $cm^2\ V^{-1}\ s^{-1}$ were extracted. When V_{gs}–V_{th} = 1 V, the position of the "hot-spot" where the current value in each layer is at maximum was at approximately ninth layer from the bottom (Figure 6c). This means that, for the current to flow, it must pass through the two or three layers of the vdW gap, and R_c at this time was as high as ≈10 kΩ μm. By contrast, when V_{gs}–V_{th} = 5 V, the position of the hot-spot was at approximately tenth layer from the bottom, and R_c was as low as ≈5 kΩ μm because it passed through a vdW gap of one or two layers. A hot-spot is formed close to the contact side when V_{gs} increases, implying a decrease in R_c.

When the thickness of MoS_2 increases, the charge distribution becomes biased to the source and drain electrodes. If there is no R_{int}, a decrease in CI screening results in a saturation in μ with the thickness. However, when R_{int} is present, charges nearer to the source and drain electrodes contribute more to the charge transport. Since the amount of induced charges at the upper layers becomes smaller with thickness due to Thomas–Fermi screening, the increase in thickness results in a decrease in μ. Experimentally, when μ of MoS_2 is measured by varying the thickness from 2 to 70 nm, μ_{FE} is 29 $cm^2\ V^{-1}\ s^{-1}$ at 2 nm but increases to ≈185 $cm^2\ V^{-1}\ s^{-1}$ at 10 nm, and again decreases to ≈36 $cm^2\ V^{-1}\ s^{-1}$ at 36 nm. This shows that the optimized thickness of MoS_2 for a high μ is 6–12 nm. In the case of graphene with a small λ and a small R_{int}, the charge is mostly collected at the bottom when gate bias is applied.[112a] In this case, the resistance required to access the bottom layer is small, and thus the hot-spot is mainly located at the bottom. Therefore, a device with a single layer performs better than a multilayer device.

Similarly, Zheng et al. reported that by using CVD-grown pyramidal MoS_2, μ can be increased by lowering R_c.[113] The size

of the synthesized MoS_2 was 20–30 μm, with an exposed edge width of 200–600 nm. Interestingly, μ of the pyramid structure was at least 1.4-fold (four layers) to up to fivefold (one to three layers) larger than that of exfoliated samples with the same thickness. This is because the electrodes are in contact with the edges of each layer, allowing electrons to be transferred to the lower layer without overcoming the interlayer resistance (R_{int}).

Li et al. proposed a model for a lopsided carrier concentration distribution, as previously proposed for Si and GaAs, to describe the CI scattering with the thickness of the MoS_2 (Figure 6d).[114] The concentration distribution is a function of V_g and the thickness. According to this function, as the thickness of the MoS_2 increases in the back-gated structure, the charge is dispersed and the peak point of the charge concentration moves away from the gate. At this time, because the Coulomb scattering rate is inversely proportional to the square of the distance, CI scattering decreases when the thickness increases. In addition, as V_{gs}–V_{th} increases, the carrier is distributed closer to the gate, and thus the CI scattering is reduced; however, as the Fröhlich scattering by the longitudinal optical phonons (48 meV) increases, μ increases initially but soon reached to the saturation (Figure 6e and polar optical phonon in Figure 6f).[115] At this time, when the MoS_2 is thin, the effect of the CI is significant, and thus the V_{gs}–V_{th} required for CI shielding becomes extremely large. Therefore, it can explain that μ is not saturated within the limited range of V_{gs}–V_{th}. By contrast, the authors evaluated μ_{FE} with the number of layers while varying the gate position and the GIs in a double-gate device. In a bottom-gate device, when the top-gate GI is HfO_2, μ_{FE} in a single layer increased by approximately twofold compared with that in air. However, as the number of layers increases, the upper part of the MoS_2 acts as an insulating film ($\kappa_{MoS2} = 17.8 \approx \kappa_{HfO2}$), and the effect of improving μ_{FE} by the high-κ GI is almost disappeared. In a top-gate device, the charge accumulated at the top side of MoS_2 enhances the CI shielding effect, increasing the μ_{FE} of each sample by ≈50%. However, even with the top-gate structures and high-κ GIs, the single-layer μ_{FE} increased by up to threefold, which is still several times smaller than that predicted theoretically. Therefore, the authors suggested that lowering the concentration of impurities will be more effective. Impurities are derived from gaseous adsorbates on the upper surface, residues during the device fabrication, water molecules at the interface, and unsaturated bonds of SiO_2 on the lower surface. They can be removed through a post-annealing and transfer in a dry environment. It was predicted that when the concentration of impurities is reduced by tenfold, from 3×10^{12} to 0.3×10^{12} cm^{-2}, the monolayer μ_{FE} become more than doubled.

5.2.3. Effect of Transition Metal and Chalcogen Combinations

Huang et al. predicted μ_e at room temperature by selecting 14 types of semiconducting 1T and 1H structures from layered MX_2 compounds in the International Crystal Structure Database (ICSD).[116] At this time, the charge scattering originates from LA phonon scattering (μ_{LA}), optical phonon scattering (μ_{OP}), and piezoelectric scattering (μ_{PZ}), and it is assumed that there is no influence from impurities. Then μ can be calculated as $1/\mu = 1/\mu_{LA} + 1/\mu_{OP} + 1/\mu_{PZ}$. Piezoelectric scattering indicates scattering from an interaction of the charge and the electric field generated when a deformation occurs in a crystal without inversion symmetry (piezoelectric crystals, such as 1H-MoS_2, $MoSe_2$, $MoTe_2$, WS_2, and WSe_2). Only μ_{LA} and μ_{OP} were considered for the 1T phase crystals (HfS_2, $HfSe_2$, PtS_2, $PtSe_2$, $PtTe_2$, SnS_2, $SnSe_2$, ZrS_2, and $ZrSe_2$), which are not piezoelectric crystals. Interestingly, as the difference in atomic weight between M and X increased, energy gap between optical and acoustic branch increased, and thus scattering between acoustic and optical phonon modes are suppressed, which result in an increase in thermal conductivity. Therefore, calculated μ showed the tendency of $\mu_{MS2} > \mu_{MSe2} > \mu_{MTe2}$. For example, the predicted μ of MoS_2 at room temperature was 354 $cm^2\ V^{-1}\ s^{-1}$. However, WS_2 was 1793 $cm^2\ V^{-1}\ s^{-1}$, PtS_2 was 3942 $cm^2\ V^{-1}\ s^{-1}$, and $PtSe_2$ was 4038 $cm^2\ V^{-1}\ s^{-1}$, which are approximately five to ten times higher than those of MoS_2. Because these compounds have a band gap of 1.2 to 2.0 eV, I_{on}/I_{off} is also expected to be excellent. In addition, even in an undiscovered phase and ternary or quaternary compounds, there is a possibility that a layered 2D TMDC materials having a high μ and a moderate band gap exist. For this reason, the prediction of μ of these new materials has an important meaning.

5.2.4. Effect of Doping

One of the most important, but usually a poorly considered doping source is a dielectric. A dielectric can modulate the charge density in the channel layer owing to the presence of dipoles. This effect is particularly pronounced when the dielectric is non-stoichiometric. Rai et al. reported that when TiO_x ($x < 2$) is used as GI, the R_c decreases from 2.9 to 180 Ω μm owing to the n-doping effect by GI, and μ_{FE} increases from 24 to 83 $cm^2\ V^{-1}\ s^{-1}$.[117] Here, GI was amorphous TiO_x ($x \approx 1.5$ according to XPS analysis) prepared by sol–gel method. When analyzing the photoluminescence (PL) spectrum after depositing TiO_x on MoS_2, the exciton peak decreases in intensity and red-shifts. This is typically observed when the electron concentration of MoS_2 increases because excitons formed through photo-excitation are easily converted into negatively charged trions, which are more stable and have lower energy than excitons. Therefore, it can be inferred that TiO_x has an electron donating effect. An analysis of the transfer curve shows that V_{th} negatively shifts and the gate modulation significantly decreases, which also means an increase in the electron concentration from n-doping. Similarly, Kang et al. reported that in the case of a back-gated device based on MOCVD-MoS_2 with HfO_2 as an passivation layer and SiO_2 as GI, μ_{FE} is 0.3 $cm^2\ V^{-1}\ s^{-1}$ when measured at atmospheric pressure.[88a] However, μ_{FE} improves to 12.4 $cm^2\ V^{-1}\ s^{-1}$ after the device was left in a vacuum for 10 h, and μ_{FE} is 15.8 $cm^2\ V^{-1}\ s^{-1}$ when it annealed in a vacuum for 24 h, which was explained by the doping effect from HfO_2.

Meanwhile, doping can also be achieved using a reducing/oxidizing agent that can donate or withdraw the charges. Kiriya et al. showed that doping is possible when using benzyl viologen (BV).[118] The CB edge of MoS_2 (0 V vs a standard hydrogen electrode) and the reduction potential of BV (–0.79 V for BV^0/BV^+, –0.33 V for BV^+/BV^{2+}) are located close together

such that electrons can be easily transferred from BV to MoS_2. The transfer curve has an I_{on}/I_{off} of 10^5 and R_c of 3.3 kΩ μm before doping, however, the V_{gs} dependence of I_{ds} disappears after doping. That is, degenerate doping occurs in MoS_2, where μ_{FE} is 24.7 $cm^2\ V^{-1}\ s^{-1}$, the charge density is 1.2×10^{13} cm^{-2}, and the R_c becomes approximately three times smaller (1.1 kΩ μm). The doping by BV makes almost no changes in the transfer characteristics even if the device is left in the air for 9 days. This is advantageous in terms of stability and doping level control in that BV can be reversibly removed in toluene.

A doping method using vacancy-anchored molecules was devised, which considers the presence of chalcogen vacancies on the surface of the TMDC. Sim et al. proposed a charge transfer doping using thiol molecules, which has -CF_3 (1H, 1H, 2H, 2H-perfluorodecanethiol, FDT) or -NH_2 (2-mercaptoethylamine, MEA) at the opposite side of -SH.[119] In general, -NH_2 acts as an electron donating group by lone pair electrons of N, and -F acts as an electron withdrawing group owing to its strong EN. When MEA is applied to pristine MoS_2, an -NH_2 group donate electrons to MoS_2. At the same time, it assists the adsorption of O_2 and H_2O, which act as a p-dopant. Without annealing, the two opposite effects are canceled out, and thus the transfer curve does not change significantly. However, after annealing at 250 °C for 1 h under air, in the MEA-treated sample, V_{th} shifted significantly to the left (a negative shift) and I_{on} was greatly improved, and the charge carrier density increased to 3.7×10^{12} cm^{-2}. However, when FDT was treated, V_{th} shifted to the positive, and I_{on} decreased significantly as the carrier density decreased by 1.8×10^{11} cm^{-2}. Although thiol-based doping is a stable method, there is a disadvantage in that the surface roughness increased.

Other than charge transfer doping and vacancy passivation doping, various types of doping methods are available by using $AuCl_3$,[120] alkali metal,[121] metal carbonate,[122] and plasma treatment.[123] However, except for the doping by dielectrics, most are not permanent and the effect of doping significantly reduced over time.

5.3. Contact Resistance in TMDC TFTs

5.3.1. Origin of Fermi Level Pinning

μ of TMDCs predicted by the theoretical models is high enough for display TFTs, however, the value is much lower in an actual device. Among many origins, R_c is known to play major roles in μ degradations. In Section 2.2.2, it was shown that R_c of a-Si:H and LTPS can be significantly reduced by inserting a highly doped area between the source/drain electrode and channel. However, in the case of atomically thin TMDC, it is not easy to achieve a permanent doping, and thus the metal comes into direct contact with the TMDC. In this case, as the wave function of the metal is extended to the TMDC by metal-induced gap states (MIGS), strong FLP is observed. As a result, regardless of the contact metal, Schottky barrier is formed at the interface between TMDC channel and metal electrode (**Figure 7**a,b).[24,124]

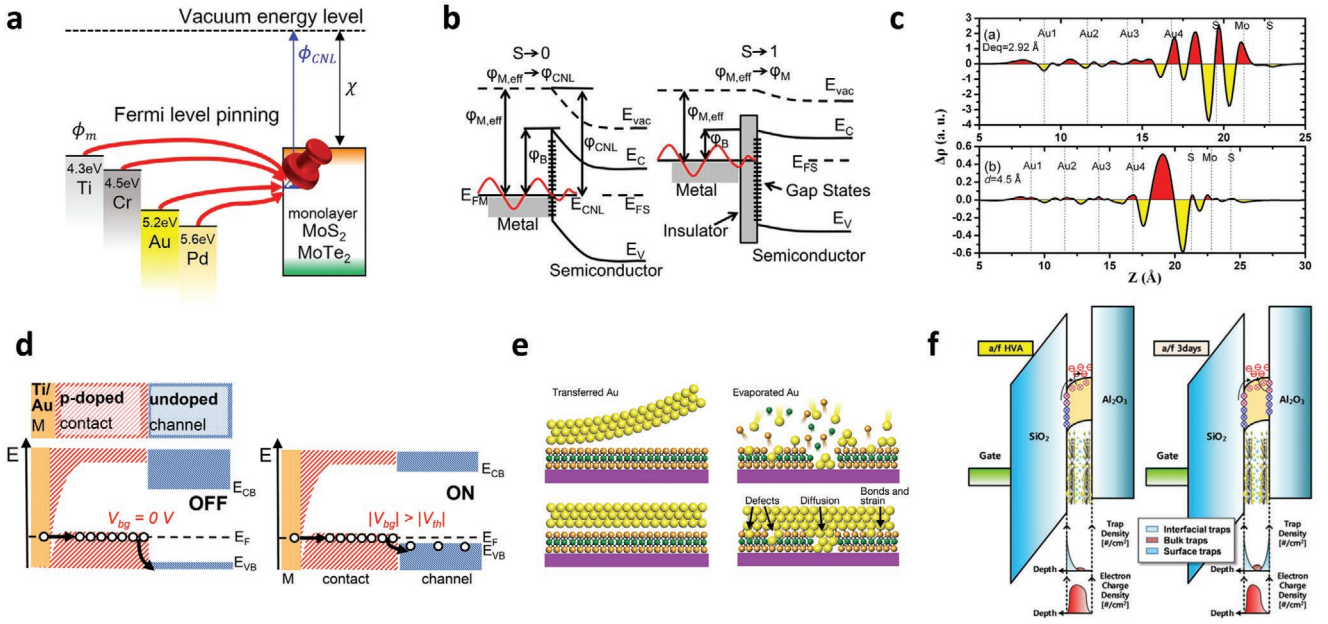

Figure 7. a) Schematic of FLP at the interface of TMDCs and metals. b) Band diagram showing strong FLP ($S \approx 0$) and FLDP ($S \approx 1$) at the metal-semiconductor junction by MIGS. E_C, E_V, and E_{vac} represent the energies of the CB edge, VB edge, and vacuum, respectively. At $S \approx 0$, E_F of metal (E_{FM}) is pinned to the charge neutrality level (E_{CNL}). If the depinning layer is inserted ($S \approx 1$), the decaying wave function of the metal cannot penetrate into the semiconductor; thus, the creation of MIGS is hindered. c) Unusual charge distribution of atomically thin TMDCs with metal contact. d) Band diagram of WSe_2 TFT with degenerate p-doped layer inserted between a metal and WSe_2. e) Schematic of vdW contact to establish FLP-free contact. f) A schematic model for explaining the layer-dependent hysteresis in multilayer MoS_2. a) Reproduced with permission.[124a] Copyright 2017, American Chemical Society. b) Reproduced with permission.[124b] Copyright 2014, AIP Publishing LLC. c) Reproduced with permission.[126] Copyright 2014, American Chemical Society. d) Reproduced with permission.[127] Copyright 2016, American Chemical Society. e) Reproduced with permission.[129] Copyright 2018, Springer Nature. f) Reproduced with permission.[139] Copyright 2016, IOP Publishing.

This is also the cause of the conduction polarity that appears regardless of the type of metal electrode. For example, in MoS_2, pinning occurs near the VB edge and thus it typically represents an n-type conductivity, and in WSe_2, pinning occurs near the CB edge, which usually shows an ambipolar characteristics owing to narrow band gap or a p-type conductivity.[125]

Meanwhile, Gong et al. argued that in addition to MIGS, the intrinsic mechanism that appears between 2D semiconductors and metals also contributes to the FLP.[126] To prove this, a DFT calculation was performed for the contacts between several metals and MoS_2. The model assumed that MoS_2 is pristine without any defects. Therefore, MIGS or defect-induced gap states (DIGS) mechanism could not contribute to FLP. Figure 7c shows the plane-averaged charge density difference ($\Delta\rho$) with the distance before and after the contact is made. Change in the dipole moment can be obtained by integrating $\Delta\rho$ multiplied by distance with the distance, and the result indicates that the dipole moment at the interface was induced by the contact between metal and MoS_2. This is due to the small space available for an atomically thin MoS_2 to accommodate the electrons, and thus the dipole greatly reduces effective φ of metal by rehybridizing the metal d orbitals. In this case, as the distance between the metal and MoS_2 increases, the dipole moment induced at the interface is reduced. Therefore, inserting a buffer layer between metal and MoS_2 can be effective to mitigate FLP. Meanwhile, at the interface, atoms from metal electrode and sulfur ($S_{contact}$) on the surface of the MoS_2 can form a bond. Therefore, the bond between the $S_{contact}$–Mo is weakened. Accordingly, Mo d states in the band edge become spread within the band gap to form a gap state, which also contributes to FLP. In this case, the gap state exists locally in Mo instead of $S_{contact}$, which cannot be explained by decaying wave function with the distance from the metal (MIGS). As a result, the pinning factor (S) was calculated as 0.71, which indicates a weak pinning. Here, S is defined by the first-order partial derivative of SBH with respect to φ, or the change of SBH with φ. In the case of Al, because the d band exists deeper than the s and p bands, the direction of the induced dipole moment is different from that of other metals (Ag, Au, Pd, Ir, and Pt), which increases φ. In addition, if the d orbital is full (Ag, Al, and Au), the interaction with MoS_2 is relatively small, and thus the shift in the E_F of MoS_2 with the metal contact is small. In the case of Pt, large φ (6.1 eV) lead to a p-type conduction in MoS_2.

5.3.2. Contact Engineering by Work Function Engineering of Metals

Das et al. reported that μ_{FE} is obtained differently depending on the type of metal when using Sc (φ = 3.5 eV), Ti (φ = 4.3 eV), Ni (φ = 5.0 eV), and Pt (φ = 5.9 eV) as electrodes of a ten-layer MoS_2.[94] Here, using Richardson equation, SBH (30 meV for Sc, ≈50 meV for Ti, ≈150 meV for Ni, and ≈230 meV for Pt) was extracted from the V_{ds}–I_{ds} relationship with temperature. This differs from the SBH estimated from the subtraction of φ to the χ of MoS_2, which is attributed to FLP. At this point, S obtained was 0.1, which indicates that a strong pinning occurred. As a result, μ_{FE} was obtained as 184 $cm^2\ V^{-1}\ s^{-1}$ for Sc, 125 $cm^2\ V^{-1}\ s^{-1}$ for Ti, 90 $cm^2\ V^{-1}\ s^{-1}$ for Ni, and 21 $cm^2\ V^{-1}\ s^{-1}$ for Pt. That is, the value of μ_{FE} was higher when the SBH is lower.

Chuang et al. reported that p-type conductivity can be achieved in MoS_2 when using MoO_x ($x < 3$) with a high φ (6.6 eV).[125] Although MoO_x has a high resistivity of ≈200 Ω μm, depositing a sufficiently thin MoO_x layer of 50 nm or less results in the carrier transport without hindrance. Meanwhile, an XPS analysis of Pd (φ = 5.1 eV) and MoO_x showed that the Pd has a sharp Fermi–Dirac step near the VB edge, whereas MoO_x has relatively weak defect bands by weak O-vacancies near the VB edge. This means that MoO_x not only has a low DOS near the E_F but also has localized bonding states, which greatly reduces the formation of MIGS. Therefore, MoO_x is less affected by the FLP and different to MoS_2 contacted with high φ metal (e.g., Pd) showing an n-type conduction, MoS_2 contacted with MoO_x shows a p-type conduction.

Chuang et al. achieved a low R_c of ≈300 Ω μm by inserting a degenerate p-doped MoS_2 ($Mo_{0.095}Nb_{0.005}S_2$) layer between the metal electrode (Ti/Au) and WSe_2.[127] At this time, the doped layer was grown using the chemical vapor transport, and shows good environmental and thermal stability because Nb is connected by a covalent bond. Meanwhile, the difference in carrier density between the doped MoS_2 and bare MoS_2 establishes a band offset (Figure 7d). In traditional 3D semiconductors, the band offset is determined by a covalent bond between the two materials. In the case of junctions between 2D materials, weak interlayer binding energy makes the control over the energy band of bare MoS_2 channel possible by applying gate bias without altering the energy level of doped MoS_2 layer. That is, control of the band offset by tuning gate bias is possible. In this way, SBH for hole injection and the R_c was greatly reduced, and an ohmic contact with the μ_{FE} of 220 $cm^2\ V^{-1}\ s^{-1}$ was achieved.

5.3.3. Contact Engineering by Inserting Fermi Level Denning Layer

Kim et al. validated the Fermi level depinning (FLDP) effects in a more systematic way by introducing a buffer layer.[128] TiO_2 was used as a buffer layer, where TiO_2 was deposited only in the source and drain area, excluding the effects of the interaction between the channel and the buffer layer. In addition, both source/drain and source/buffer/drain structures were implemented on the same exfoliated single crystal MoS_2, eliminating the effects of changes in the characteristics of the channel materials. At this time, Ti, Cr, Au, and Pt electrodes were used, and devices with these metals showed n-type conductions. Interestingly, for Ti, there was little change in I_{on} owing to the insertion of 1 nm TiO_2. However, I_{on} decreased by tenfold for Cu, 10^2-fold for Au, and 10^3-fold with Pt. Since I_{on} decreases as the φ of the metal increases, it can be inferred that the SBH for electron notably increased with metal φ by the FLDP. Meanwhile, when fitted using thermionic emission model, S was found to be increased from 0.02 (metal/MoS_2 structure) to 0.24 (metal/insulator/MoS_2 structure) with a TiO_2 layer insertion. For the thickness of the TiO_2, the SBH tends to increase with the buffer layer thickness, which means an increased FLDP with the buffer layer thickness. Meanwhile, the FLDP can be induced by 1) MIGS reduction, 2) metal/semiconductor interface passivation, and 3) a dipole formation at the interface. To

evaluate this, the SBH of an electron was plotted as a function of metal φ. The SBH at the intersection between the real metal/MoS_2 contact ($S = 0.02$) and an ideal metal/MoS_2 contact ($S = 1$) was calculated as 45 meV. For a perfect pinning ($S = 0$), the line also shares the same intersection point with $S = 0.02$ and $S = 1$. In an ideal case, SBH is 0 for perfect pinning. Therefore, the discrepancy indicates that the pinning point within the multilayered MoS_2 band gap, or E_{CNL}, is located 45 meV below the CB edge. Based on these results, when $S = 0.24$ without influence from dipole (crossing the common intersection point) is compared with the experimental data for metal/TiO_2/MoS_2, the SBH reduction owing the formation of the dipole was estimated as 38 meV. Meanwhile, the deposition of TiO_2 by sputtering makes the surface of MoS_2 worse than that of the pristine MoS_2, and thus the effect of interface passivation by TiO_2 insertion is negligible. Therefore, the authors concluded that FLDP owing to an introduction of a buffer layer is mainly caused by a reduction of the MIGS, and the formation of dipoles makes a minor contribution.

5.3.4. Achieving van der Waals Contact for Weak Fermi Level Pinning

Since strong FLP in TMDCs occurs by the interactions between metals and TMDCs (e.g., formation of hybrid bonds), it is important to achieve vdW contact between metals and TMDCs that the SBH can be tuned as designed. Lie et al. reported that vdW contacts at the interface can be achieved by transferring metal electrodes onto the MoS_2 (Figure 7e).[129] In detail, a metal pattern was formed on a Si substrate and transferred to a multilayer MoS_2(4–20 nm)/PMMA/SiO_2/Si substrate using PDMS. After that, only PMMA on the contact pad was removed and the transport characteristics were measured. Analysis of the device by cross-sectional TEM shows that the MoS_2/metal interface is atomically sharp when the metal electrodes were transferred by PDMS. Contrary to this, in the case of direct metallization by electron beam evaporator, defects, strain, disorder, and metal diffusion were observed at the interface. In terms of conductivity, devices with Ag ($\varphi = 4.3$ eV) electrode showed n-type, and devices with Cu ($\varphi = 4.6$ eV) showed a bipolar characteristics but more like an n-type with I_{ds} three orders of magnitude smaller than the device with Ag electrode. This indicates that Cu has larger SBH for electron than Ag. Devices with Au ($\varphi = 5.1$ eV) and Pt ($\varphi = 5.9$ eV) electrodes exhibited a p-type conductivity due to the high φ, while the conductivities are n-type in the case of direct metallization due to FLP. Calculation of S value showed that the direct metallization has S value of 0.09, indicating strong FLP. On the other hand, when the metal electrode was transferred, S was obtained as 0.96, indicating almost no FLP is present. For the devices fabricated by metal electrode transfer method with PMMA/SiO_2 as GI, μ_{FE} of MoS_2 was obtained as 260 $cm^2\ V^{-1}\ s^{-1}$ for electrons (Ag electrode) and 175 $cm^2\ V^{-1}\ s^{-1}$ for holes (Pt electrode) at room temperature. For serial tunneling resistance established by vdW gap, the authors concluded that the contribution is negligible (theoretically estimated as 10^{-10}–10^{-8} $\Omega\ cm^2$) due to very small gap (0.10–0.14 nm for theoretical predictions and 0.15 nm for experimental measurement). For reference, R_c in MoS_2-based TFTs is in general 10^{-5}–10^{-3} $\Omega\ cm^2$.

Similarly, Jung et al. used transferred via contact (TVC) method to realize vdW contact between metal and TMDCs.[130] Different to the previous report, metal electrode was dry transferred by h-BN, which has an advantage of preventing interfacial contamination by polymer residues. For carrying out TVC method, the environment was found to be very important. When the TVC is conducted within a glovebox, Pt/2L WSe_2 device exhibited mainly a p-type conduction with V_{th} of ≈20 V, and a weak n-type conduction with V_{th} of ≈30 V. At 295 K, μ_{FE} for hole was 195 $cm^2\ V^{-1}\ s^{-1}$ and an R_C was 3.5 kΩ μm. By contrast, when the TVC is performed in the air, V_{th} was negatively shifted (–10 V) for both p- and n-type conduction and I_{on} for the p-type conduction was significantly reduced. This indicates that contamination by water and hydrocarbons occurs when the device is exposed to air, which moves E_F of the metal toward the mid-gap of the WSe_2, increasing the SBH for a hole injection. In addition, due to charge trapping at the interface, hysteresis is also observed.

Meanwhile, Wang et al. showed that a vdW contact can be made by using a soft metal, which does not damage the surface of MoS_2 during the deposition process.[131] To demonstrate the concept, In (10 nm) was first deposited at 10^{-6} torr and then Au (100 nm) as a capping layer was deposited to prevent oxidation of In in the air. When the device with vdW contact was fabricated, R_C was 3.3 kΩ μm at a single layer and 800 Ω μm at a multilayer MoS_2. μ_{FE} was measured as 167 $cm^2\ V^{-1}\ s^{-1}$ despite the use of SiO_2 as GI and the channel remaining unencapsulated. At this time, the SBH was found to be 110 meV, which is the difference between φ_{In} (4.1 eV) and χ of MoS_2 (4.0 eV), which indicates that FLP does not occur at the interface. Unlike MoS_2, WS_2 and WSe_2 have barriers to the electron or hole injection and thus have a high resistance because the CB or VB edge does not match well with φ_{In}. For WSe_2, the electronic injection barrier is 0.60 eV ($R_C = 16$ kΩ μm) and the hole injection barrier is 0.73 eV ($R_C = 225$ kΩ μm) when In/Au is used as an electrode. In this case, however, charge injection barrier can be controlled by deposition of alloys of In and other metals. Soft nature of In metal is suitable for the alloy formation. For example, when In (3 nm)/Pt (100 nm) was used as an electrode, the Kelvin force microscopy (KFM) measurement showed that φ of metal slightly increased from 4.05 (In) to 4.23 eV (In/Pt).

Kim et al. demonstrated a vdW contact by evaporating metal at a moderately low temperature, and at the same time, the substrate is cooled to 100 K using liquid nitrogen.[132] When the interfaces of In or Au-deposited MoS_2/SiO_2/Si were analyzed by TEM, Au was found to invade MoS_2 and make defects on the first and second layer of MoS_2, while In make a clean interface without invasion. This is because In melts at ≈530 °C at the deposition pressure of 10^{-7} torr, whereas Au melts at ≈860 °C that makes evaporating Au clusters more energetic. In the case of the substrate temperature, the film was uniformly deposited at a low temperature (100 K), while granular film was deposited at room temperature. This suggests that lowering the energy of the metal cluster near the substrate is also important. Based on this, 6L MoS_2 devices with In as source and drain electrodes, SiO_2 as the GI, and h-BN as an encapsulation layer, showed μ_{FE} of 50 $cm^2\ V^{-1}\ s^{-1}$ and an R_C of 1 to 2 kΩ μm at room temperature. At this point, the R_C

decreased as the temperature decreases, implying ohmic contact is established.

5.4. Effect of Fabrication Processes on the Performance of TMDC TFTs

5.4.1. Effect of Metal Deposition Pressures

Different to the predictions, the real devices typically show μ below the expectations. When handled without care, there are possibilities that the samples are degraded in the ambient conditions. Also, there are some chances that the degradation occurs during the deposition process. McDonnell et al. confirmed that when depositing Ti on MoS_2, different interfaces are formed depending on the deposition pressure.[133] Here, the formation energies of the compounds possibly made during the deposition are −890 kJ mol^{-1} for TiO_2, −226 kJ mol^{-1} for MoS_2, and −574 to −390 kJ mol^{-1} for TiS_x. Under a high vacuum (HV, $\approx 7.5 \times 10^{-7}$ torr), Ti can be oxidized while it is deposited since O_2 is sufficient. XPS analysis also confirmed the formation of TiO_2. Under ultra-high vacuum (UHV, $\approx 7.5 \times 10^{-10}$ torr), TiO_2 could not be formed owing to a low O_2 concentration. Rather, TiS_x is formed that is energetically more stable than MoS_2. Also, Mo and Mo_xS_y are formed as by-products. When the samples are passivated by 2 nm of Au during deposition, oxygen was not detected at samples with Ti deposited under UHV, while it was not at the samples with Ti deposited under HV. Therefore, TiO_2 formed under HV originated from the deposition process, not from oxidation after deposition. At this time, due to the similar value for χ of TiO_2 and φ_{Ti}, the electrical characteristics are not significantly altered when TiO_2 is deposited instead of Ti.

Meanwhile, English et al. argued that there may be differences in the device performance depending on the deposition pressure of the metal electrode.[134] When the morphology of metal is compared, UHV (10^{-9} torr) deposited Au showed sub-micrometer granules whereas HV (10^{-6} torr) deposited Au had nanocrystalline granules. Since the amount of adsorbed adsorbates at the metal-MoS_2 interface at UHV is small, Au-MoS_2 binding energy becomes smaller than cohesive energy of Au. This prefers to have a larger grain size for Au when deposited at UHV. As a result, MoS_2-Au interface can be smoother, which reduces R_C and increases μ. In addition, the reduced amount of adsorbates at the interface also suppresses CI scattering, decreasing the R_C and increasing μ. Consequently, the R_C was reduced by approximately threefold by depositing Au under UHV rather than HV. Meanwhile, the effective barrier height extracted from the Richardson equation was not significantly different between UHV-Au and HV-Au, which implies that R_C rather than the SBH has a major effect on the device performance.

5.4.2. Effect of Process Residues

Atomically thin TMDCs are vulnerable to any residues left during the device fabrication process. This is because the space that can accommodate changes by the residues (e.g., transferred charge) is relatively small. Liang et al. argued that PMMA as a typical photoresist cannot be completely removed even through vacuum annealing is carried out. The left PMMA acts as a p-type dopant and induces a carrier density of 7.2×10^{11} cm^{-2}.[135] At this time, if the remaining PMMA is removed by scanning the surface of the TMDC in contact mode AFM, the surface roughness is reduced from 1.11 to 0.33 nm, and the maximum drain current increased by 136% on average and μ_{FE} increased by 13%. Along with the photoresist, heterogeneous seed (e.g., PTAS) during the CVD process can also affect to μ. Utama et al. reported that PTAS acts as an impurity source and can worsen the electrical characteristics by increasing the roughness scattering.[98] For two to five layered MoS_2, μ of MoS_2 grown without PTAS ($\approx$1–10 cm^2 V^{-1} s^{-1}) was more than three orders of magnitude larger than MoS_2 grown with PTAS ($\approx 10^{-3}$ cm^2 V^{-1} s^{-1}).

5.4.3. Effect of Strain

If the growth of TMDC is assisted by the thermal energy, a strain is inevitably generated in the as-grown TMDC during substrate cooling owing to differences in the thermal expansion coefficients between the TMDC and substrate. Atomically thin TMDC is vulnerable to the change in its properties by the strain, which also affects to the electrical characteristics. Amani et al. compared the properties of as-grown CVD-MoS_2 and CVD-MoS_2 transferred to a new substrate.[136] When measuring the length of the edge directly by scanning electron microscopy, it was found that a 1.24% tensile strain is applied to the as-grown MoS_2. This was similar to the value of the tensile strain of 1.37% calculated from the $E_{2g}{}^1$ and A_{1g} peak shifts in the Raman spectra. Meanwhile, when the strain is released by transfer process, μ becomes 17.6 cm^2 V^{-1} s^{-1}, which is three times larger than the as-grown MoS_2 (5.0 cm^2 V^{-1} s^{-1}).

5.5. Reliability of TMDC TFTs

5.5.1. Hysteresis

Hysteresis in display TFT is important since the driving current in OLED can change significantly depending on the sweep direction and rate of gate bias. English et al. reported that the hysteresis can be reduced by evaporating adsorbates on the surface of the MoS_2 channel by vacuum annealing ($\approx 10^{-5}$ torr, 300 °C, 3 h) of devices within a probe station. At this time, I_{ds} also increased. This was attributed to a V_{th} reduction, and not an R_C reduction.[134] Indeed, from the estimation of R_C, the Au electrode did not made significant change in R_C, while Ni electrode made an increase in R_C by ≈25% as affected by oxygen during the annealing process.

Tongay et al. reported that the electronic concentration of MoS_2 can be controlled by the adsorption of O_2 and H_2O from the air onto the surface of MoS_2.[137] Here, O_2 and H_2O withdraw electrons from MoS_2, and thus electrostatic screening by electrons is weakened. As a result, the exciton becomes stabilized due to an increase in the exciton binding energy. Also, as the concentration of the electrons decreases, Auger recombination and non-radiative decay is reduced. This leads to an increase in the PL intensity by ten- or 35-fold (compared to the

intensity measured at vacuum) when MoS_2 is exposed to O_2 or H_2O. Meanwhile, when one O_2 or H_2O molecule is physisorbed onto the surface of one unit cell of MoS_2, the DFT calculation showed that 0.04 (equivalent to 5×10^{13} cm^{-2} in MoS_2) and 0.01 electrons per unit cell are transferred to the adsorbates. At this time, the binding energy between the adsorbates and MoS_2 is as weak as 70–140 meV (thermal energy at room temperature is 26 meV), then the adsorption at room temperature could be reversibly controlled through gas pressure control. On the other hand, chemisorption was found to be difficult to occur due to the high energy barrier of ≈2 eV. Meanwhile, the adsorbates can be anchored more strongly on the S vacancies, where the binding energy is estimated as 110 meV for O_2 and 150 meV for H_2O. At this time, the transferred charge to H_2O increased by fivefold. However, such responses were not observed in inert gases, and a forming process was necessary to obtain sensitive responses. At this time, annealing is likely to remove contaminants or organic residues, to relieve stress built between the substrate and MoS_2, or to form chalcogen vacancies. Similarly, Schmidt et al. reported that when back-gated MoS_2 device with its surface exposed to air was annealed at 200 °C for 2 h in a N_2 atmosphere, there were no changes in the transfer curve. However, a subsequent annealing at 120 °C in vacuum for 4–10 h make a negative shift in a transfer curve owing to the desorption of O_2 and H_2O that make the device more n-type.[138]

Yu et al. evaluated hysteresis behavior depending on the number of MoS_2 layers (Figure 7f).[139] Interestingly, bilayer MoS_2 passivated by ALD-Al_2O_3 showed no hysteresis after passivation. It followed conventional carrier number fluctuation model in $1/f$ noise models. However, for multilayer, it exhibited large hysteresis even if it was passivated. From $1/f$ noise analysis, the authors found that the frequency behavior does not follow well-known $1/f$ noise models because of bulk traps inside the MoS_2. From SIMS profiling, they found that oxygen species exists in the exfoliated MoS_2 and suggested that such oxygen species contribute as bulk trap sites.

5.5.2. Environmental Stability

In general, TMDC shows a deterioration of the surface even when exposed to air for a short period of time. Gao et al. measured the properties of CVD-WS_2 after it is stored in ambient conditions for a year.[140] As a result, most areas of the WS_2 disappeared in the optical image, and the PL intensity was reduced by up to sixfold. In addition, even when CVD-WS_2 was stored at ≈1 torr for 1 month, two orders of magnitude reduction in the drain current is observed. From XPS analysis, W:S = 1:1.33 was measured. Also, as the sample is aged, S losses become notable and the amount of W-O bond increased. Meanwhile, from the Auger electron spectroscopy element mapping, oxygen was found to be rich at the grain boundaries and edges. From the fact that single crystal mechanically exfoliated samples showed low degradation rate over time, the authors suggested that oxidation through aging occur in the following sequence: 1) initiation of oxidation at the crystal edge, grain boundary, and defects (e.g., vacancy). 2) Propagation of oxidation to the grain interiors. Such degradations can be suppressed by coating the barrier layers with a low water and O_2 permeability, such as with perylene C and PMMA. Meanwhile, control over the growth conditions and growth geometry may also suppress a degradation of the synthesized sample (e.g., CVD-grown sample). For example, MoS_2 grown at a low vapor concentration did not show any apparent changes in the properties during the aging owing to its small S vacancy concentration.[141]

5.6. OLED Applications of TMDC TFTs

Recently, efforts on driving pixels in displays based on TMDC TFTs were made by several groups. Atomically thin nature of TMDCs are advantageous in realizing deformable, flexible, foldable, rollable displays and soft electronics requiring both a mechanical robustness and a high electrical performance. **Figure 8**a shows a pixel driving circuit using mechanically exfoliated WSe_2 as a channel material for switching and driving TFTs.[142] With the traditional 2T driving circuit, on and off of OLED pixels and adjusting grayscale luminance is possible. Here, a switching signal from the switching TFT (left-side TFT in Figure 8a) controls the on/off operation of the pixel driving circuit, and the data signal from the switching TFT controls the grayscale of the OLED while the switching signal is in an on-state. According to this operating mechanism of a 2T driving circuit, OLED pixels show only an on-state when the gate voltage swing (V_{SW}) and the data voltage (V_{DATA}) are simultaneously applied at 2–3 and 6–7 s (Figure 8b). Since an OLED is based on a current driving scheme, precise control over the OLED driving current (I_{OLED}) is very important. Here, I_{OLED} could be adjusted by changing V_{DATA}. When V_{DATA} was increased from −5 to −3 V, I_{OLED} decreases from 8.46 to 0.62 μA, and the luminance of the OLED also decreased (Figure 8c).

Later on, Woo et al. fabricated a 2T driving circuit for an OLED operation on a flexible plastic substrate using CVD-grown bi/trilayer MoS_2 as a channel material (Figure 8d).[143] When tested under a 2T driving scheme, both high uniformity in electrical characteristics over large area and a sufficient performance of the switching and driving TFTs were confirmed. In terms of electrical properties, I_{on} over 100 μA, I_{on}/I_{off} of ≈10^9, and μ_{FE} of ≈9 cm^2 V^{-1} s^{-1} were obtained. For a bending test with a bending radius (R) from infinite (flat state) to a 4 mm, the TFT showed a stable current density and I_{on}/I_{off}, as shown in Figure 8e. Figure 8f shows that as V_{DATA} decreased from 8 to 1 V, output current (I_{OUTPUT}) also decreased accordingly, indicating that the grayscale control is possible with high reliability even under R = 3.5 mm. This corresponds to a strong tensile strain of 1.82%, indicating a nearly critical point of an Al_2O_3 breakdown. That is, for the displays based on TMDCs, an inorganic GI can be a limiting factor in achieving high flexibility.

Similarly, Choi et al. demonstrated an AM-OLED driven by bilayer MoS_2 TFTs on a flexible polymer substrate (Figure 8g).[144] Here, MOCVD at a moderately low pressure (7.5 torr) enabled a centimeter-scale growth of MoS_2. The MoS_2 film had a high uniformity in electrical properties (over 500 TFTs) with an average μ of 18.1 cm^2 V^{-1} s^{-1}, which is sufficient

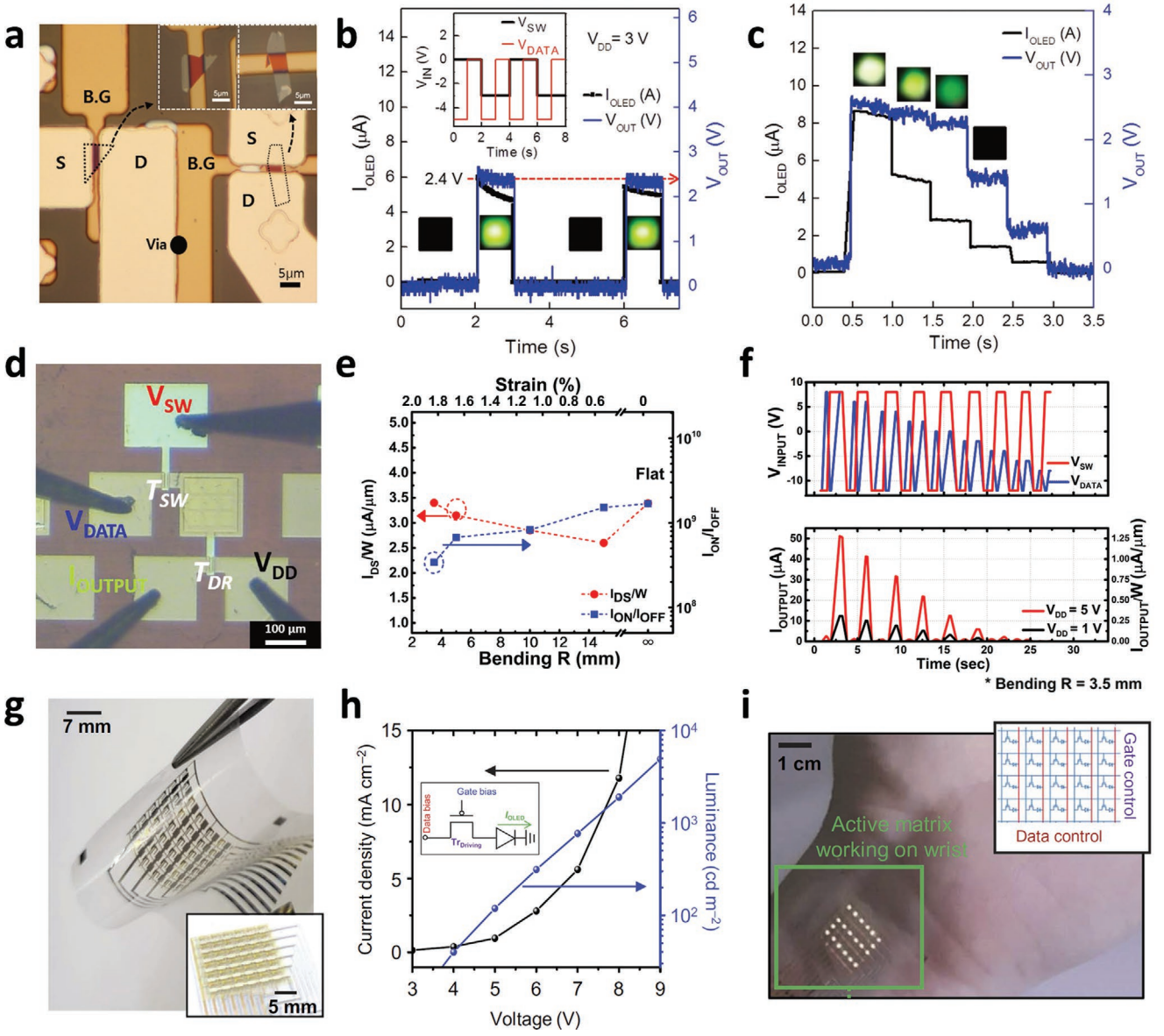

Figure 8. a) Optical image of AM-OLED pixel driving circuit using an exfoliated WSe_2 flake as a TFT channel. b) OLED pixel operation using WSe_2 TFTs in time domain under V_{DD} of 3 V. Inset shows dynamic operation by V_{SW} and V_{DATA}. c) Grayscale modulation of luminance by controlling I_{OLED}. d) 2T driving circuit on the flexible plastic substrate using CVD-grown MoS_2 TFTs. e) Current density and I_{on}/I_{off} as a function of bending radius (or strain). f) Input voltages of V_{SW} and V_{DATA} in time domain and the corresponding I_{OUTPUT} and output current density. g) Flexible AM-OLED circuit on a plastic substrate using MOCVD-MoS_2 as a channel material. h) Change in the current density and luminance with the gate bias. i) Operation of AM-OLED showing number 2 represented by pixels on a human wrist. a–c) Reproduced with permission.[142] Copyright 2016, Wiley-VCH. d–f) Reproduced with permission.[143] Copyright 2018, Wiley-VCH. g–i) Reproduced with permission.[144] Copyright 2018, AAAS.

to drive AM-OLED. However, a simple 1T-1OLED scheme is used, and thus I_{OLED} must be controlled by the gate bias under a constant data bias (Figure 8h). Finally, by controlling gate bias and data bias in real time, displaying letters of M-O-S-2 in a sequence was demonstrated (Figure 8i). Not only the display was working on a human wrist, but also its variation in I_{on}/I_{off} was very small (± 2%) without the external compensation circuits. Also, a small variation in I_{OLED} at R = 0.7 mm was shown, implying TMDCs have great potentials in realizing future displays with various form factors requiring an extreme flexibility.

6. Conclusion

Displays have evolved in such a way that they provide users more conveniences as an interactive platform of communications among people, by delivering visual information in the form of light. In early days, displays were bulky, energy-inefficient, and had low resolutions. However, the development of TFT technologies resulted in a breakthrough, realizing slim, lightweight, and high-resolution flat panel displays. Along with the development of new display types such as LCD and OLED, transitions in form factors have realized small-sized mobile

displays such as those in smart phones and smart watches, which have become an important interface in Internet of Things (IoTs) and have changed our lifestyles.

The technological transitions were made possible by the invention and development of materials and their associated device technologies. For example, the establishment of excimer laser technology was the first step toward the discovery of high μ LTPS. This resulted in the widespread use of OLED, which has shown the possibilities of transforming displays into any shape. On the other hand, simulations or design-driven approaches have enabled the commercialization of large-area displays with AOSs. Similarly, the discovery of new channel materials will make it possible to realize next-generation displays such as tomographic image-synthesized layered 3D display,[145] which requires materials with exceptionally high performances. TMDC is one of the strong candidates of such new materials since it possesses exotic properties originating from the 2D electron gas system.

For the realization of new materials, not only the material property itself but the related processes should be precisely designed. For example, LTPS technology can be adopted to improve crystallinity of new channel materials by utilizing light–material interactions, which have shown significant potential for realizing high-performance 2D materials via their exceptional capability to induce multi-physical, transient, and non-equilibrium photon reactions.[146] Similarly, as recently reported by Im et al., spot-beam laser-crystallization methods, which can mitigate the line-beam associated non-uniformity issues and reduce the cost of laser, can be applied in industrial scales.[147] Likewise, the commercialization of new materials can be achieved by utilizing the existing technologies to exploit maximum material properties. Such developments in materials preparation and processing systems along with the related software and artificial intelligence (AI) technologies in the display itself[148] would enable us to make a further leap toward a new era in the display industry.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

contact resistance, device structures, display technologies, thin film transistors, transition metal dichalcogenides

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